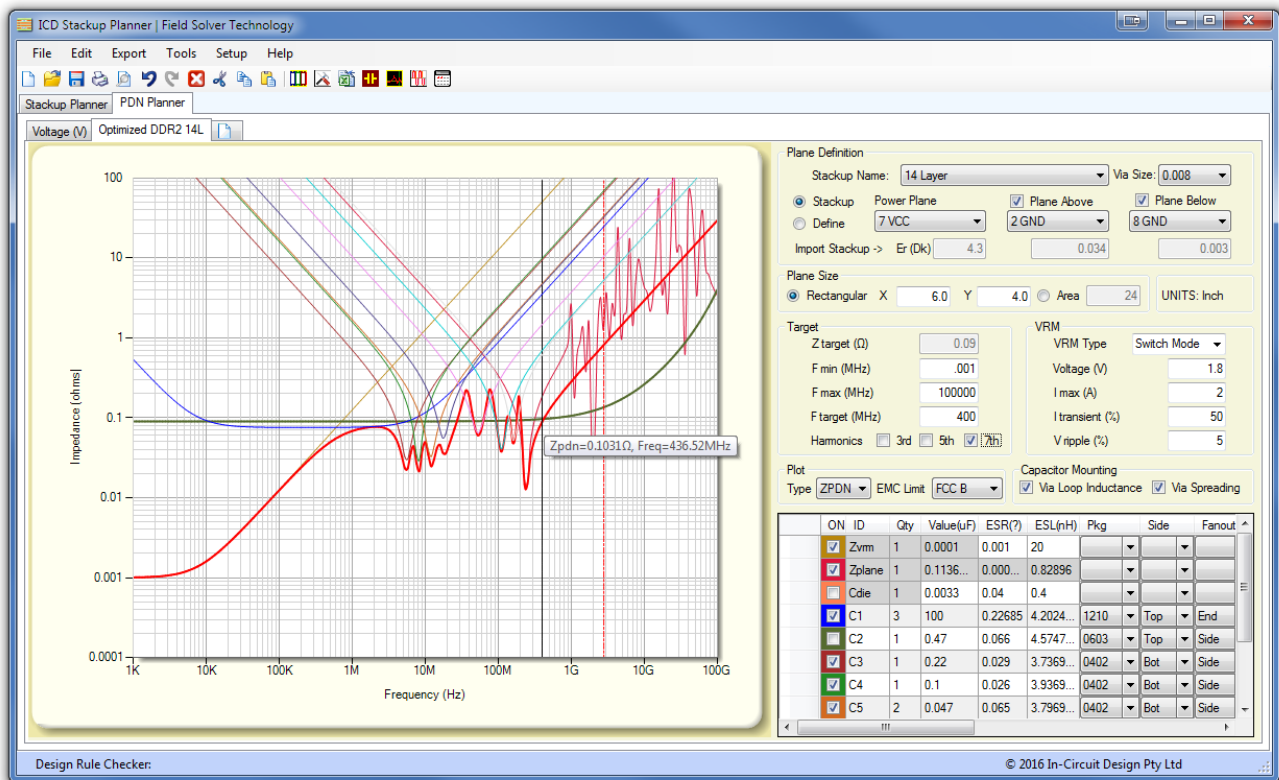# Power Distribution Network (PDN) Planner

Analyze multiple power supplies to maintain low AC impedance over the entire frequency range dramatically improving product performance and reliability

Power Distribution Network (PDN) analysis is often overlooked during the design process. Poor PDN design can result in unusual, intermittent signal integrity issues. These include high crosstalk and excessive emission of electromagnetic radiation degrading performance and reliability of the product.

PDN analysis is a relatively new addition to overall system performance simulation but its importance is now widely recognized. Traditionally, application notes and reference designs have recommended that all you need do is to add three decoupling capacitors per power pin. This is physically impossible, in most designs, due to space constraints.

If the AC impedance of a power supply is too high, at a particular frequency, the board will radiate electromagnetic emissions. Radiation is directly proportional to high AC impedance. If the impedance happens to peak at the fundamental (clock) frequency or an odd harmonic of the fundamental – 3rd, 5th or 7th then passing Electromagnetic Compliance (EMC) may be a challenge. The PDN Planner provides insight into lowering this AC impedance to an acceptable level. This all looks very complex – and it is – but all the clever math has been done making it simple for the user.
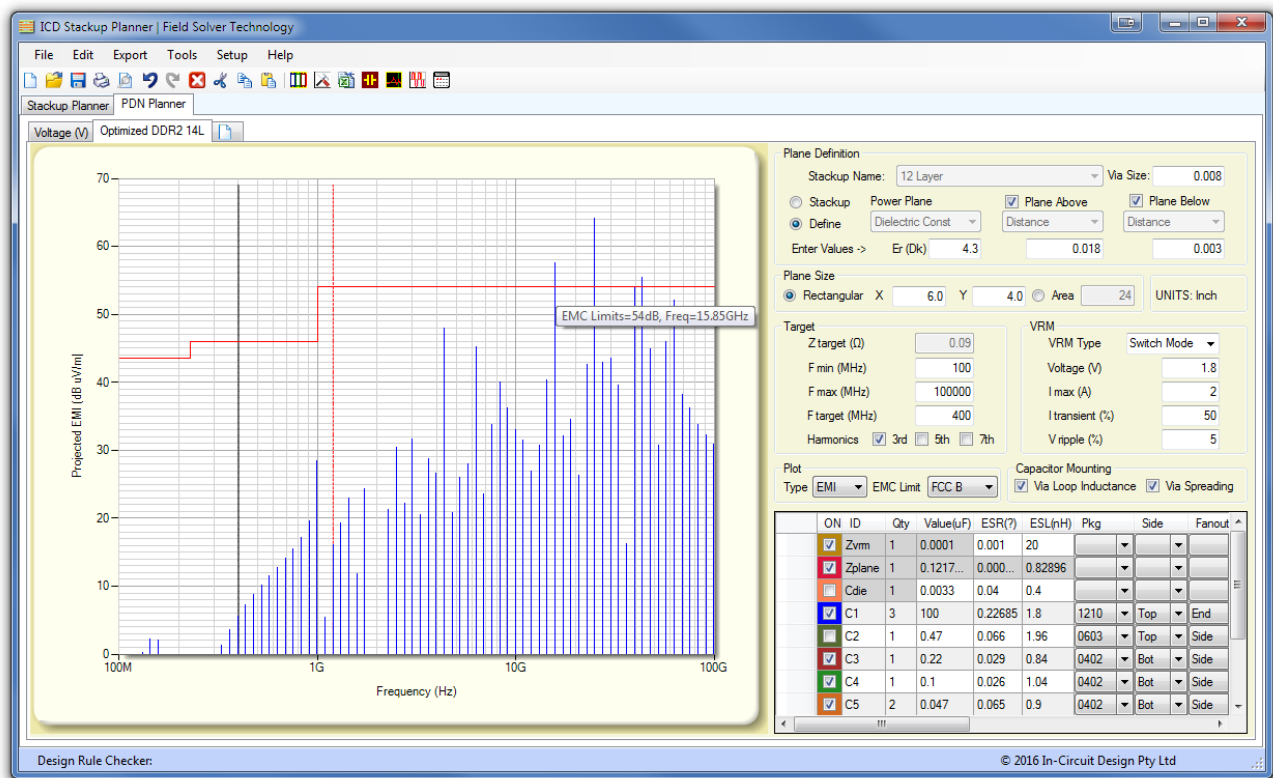
The PDN EMI plot represents the projected maximum radiated noise if a high-speed signal excites the plane resonance at a particular frequency. The applicable EMC standard can be selected from the EMC Limit pull-down menu. In Europe and Australia, the applicable EMC standard is CISPR. The United States complies to the FCC and in Japan the VCCI standard.

If the plane size is altered, then the plane resonance is shifted in frequency. A combination of modifications to dielectric thickness and dielectric constant, of the material in the ICD Stackup Planner, together with an adjustment of plane size can usually establish the minimum resonance for the configuration.

PDN Planning is a trade-off between cost/performance and:
- Gives high confidence in the performance and reliability of the product
- Meets the performance target at the lowest cost of production
- Identifies and eliminates issues early in the design cycle- saving costly re-spins

Industry-leading Ease of Use

The ICD PDN Planner builds on the familiar ease of use of the popular ICD Stackup Planner software that has been used by over twelve thousand PCB Designers and Engineers worldwide.

ICD PDN Planner allows you to analyze an unlimited number of power supply configurations simultaneously. A typical high speed, multilayer PCB has five or six individual power supplies. These all serve a different purpose, and must be regulated to maintain power integrity during high current switching up to the maximum frequency. With a frequency range up to 100GHz, the PDN Planner allows you to analyze the AC impedance of each on-board power supply network, and manage plane-resonance peaks at the odd 3rd, 5th and 7th harmonics.

The PDN Planner features:

- **Fast**—AC Analysis of an unlimited number of power supply configurations simultaneously
- **Accurate**—over 5,600 part Capacitor Library data – based on manufacturers SPICE models
- **Ease of use**—quick, intuitive, and easy to learn spreadsheet-like interface, with start-up library readily available components
- **Practical**—insert specific capacitor characteristics to simulate the effect of decoupling and bulk bypass capacitors. Takes VRM properties, plane resonance, capacitor mounting and via loop and spreading inductance into account
- **Affordable**—only a fraction of the cost of competitive tools
- **Integration**—integrated to the ICD Stackup Planner to extract plane data and location

Comprehensive Capacitor Library

A comprehensive Capacitor Library with over 5,600 readily available SMD capacitors from American Technical Ceramics, AVX, Johanson Technology, Kemet, Murata, Samsung Electro-mechanics, Taiyo Yuden and TDK and are included—listing Value, ESR, ESL, SRF, Voltage, Tolerance, Dielectric Material and SMD Package Type—and ready for insertion into PDN Planner. These libraries are extracted from the manufacturers SPICE models to ensure accuracy.

The Capacitor library features Boolean search capabilities to enable quick selection of components based on any field. You can also add your company's preferred capacitor inventory by adding specific models and saving them to a network library allowing access by fellow designers.

Plane Definition

The board stackup can be setup in the Stackup Planner first, allowing the PDN Planner to extract the plane data and locations from the stackup. The user selects their custom stackup from the list provided, and then the power and ground (GND) planes are presented for selection. Both the GND planes above and below are used to calculate the plane capacitance in a multilayer structure.

Alternatively, the user can opt to define the stackups Dielectric Constant (Er) and distance to the plane above and/or below manually. Also, plane size (if rectangular) or area (if an odd shape) can be defined. These may be quite different to the size of the board – for instance, in DDR3 design, the

1.5V plane may be only one inch square which not only affects the capacitance but also the plane resonance. As the distance between the planes approach half wave length the plane, acting as an unterminated transmission line, begins to resonate – this is displayed on both the impedance and EMI plots.
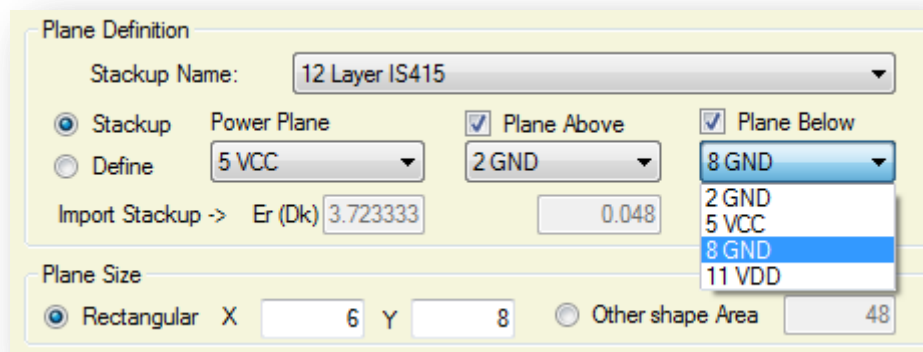

Voltage Regulator Module

The Voltage Regulator Module (VRM) is typically a switching regulator. It adjusts the amount of current being supplied (via feedback) to keep the voltage constant at frequencies from DC to a few hundred KHz (depending on the regulator). For all transient events that occur at frequencies above this range, there is a time lag before the VRM can respond to the new level of demand. Decoupling capacitors then provide current – at different frequencies – until the VRM can respond.
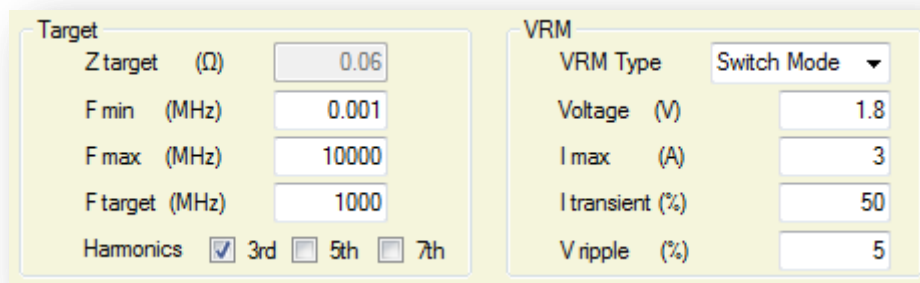
The Target Impedance – Ztarget – is determined by the rail voltage, maximum current, transient current and ripple voltage. This is calculated automatically by the PDN Planner. Once this is set, the frequency limits (minimum and maximum) and the Target Frequency – Ftarget – can be defined. The target impedance is frequency dependant. Due to the skin effect and dielectric loss, Ztarget increases with the square root of frequency from 30MHz. Ideally the PDN Impedance – Zpdn – should be below both the target impedance and target frequency. Also, markers can be placed on odd harmonics, of the fundamental frequency, to highlight peaks that may occur in this vicinity.

Capacitor List View

Capacitors are inserted into the list view from the Capacitor Library. As capacitors are added, the effective impedance of each capacitor is simulated and drawn on the impedance graph. A number of such capacitors are required for each PDN to lower the AC impedance at particular frequencies. The resultant impedance becomes the effective impedance of the PDN – Zpdn.

The package type, mounting side and fanout style are then added to each capacitor to simulate the "Via Loop Inductance" of the capacitor, land pattern, fanout inductance and via inductance. The additional inductance of the distance of capacitors to the power pins is accounted for by "Via Spreading".
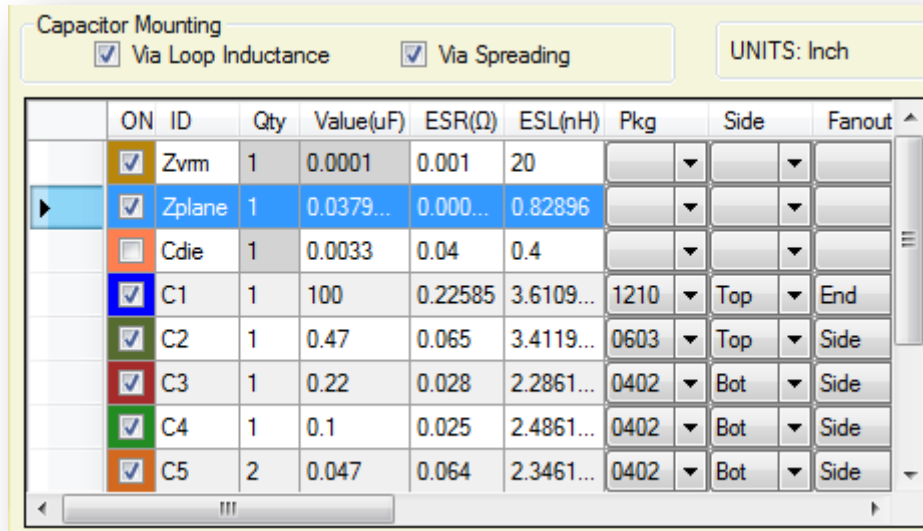
Designers can add an unlimited number of bulk bypass/decoupling capacitors. Instantly analyze the Voltage Regulator Module, PCB Substrate, capacitor mounting, via loop, and spreading inductance to determine the solution space for the effective target impedance of the Power Distribution Network.

Bill of Materials – Export to Excel

Once the PDN has been analyzed, a Bill of Materials (BOM) can be exported to Excel detailing the quantities, values, part numbers and characteristics of each capacitor used in the PDN.

Capacitor	Qty	Value (uF)	ESR (Ω)	ESL (nH)	Pkg	Side	Fanout	SRF (MHz)	Dielectric	Type	Voltage	Tol %	Land	Part Number	Comments
C1	4	100	0.22585	3.610973	1210	Top	End	0.375		TANT	6.3	20	1210	T494B107M006AT	
C2	1	0.47	0.065	3.406185	402	Bot	Side	5.246	X7R	CER	16	10	603	C0603C474K4RAC	
C3	1	0.22	0.028	2.286185	402	Bot	Side	11.714	X5R	CER	6.3	10	402	C0402C224K9PAC	
C4	1	0.1	0.025	2.486185	402	Bot	Side	15.614	X7R	CER	16	10	402	C0402C104K4RAC	
C5	2	0.047	0.064	2.346185	402	Bot	Side	24.483	X7R	CER	16	10	402	C0402C473K4RAC	
C6	3	0.022	0.10911	0.81				38.44	X7R	CER	16	10	402	C0402C223K4RAC	
C7	5	0.01	0.346	1.93				36.531	X7R	CER	50	10	402	C0402C103K5RAC	
C8	2	0.0047	0.436	1.82				54.899	X7R	CER	50	10	402	C0402C472K5RAC	
C9	16	0.0022	0.451	1.28				96.023	X7R	CER	50	10	402	C0402C222K5RAC	

Company:		**ICD PDN Planner	www.icd.com.au**
Project Name:		**Fabricator:**
Designer/Email:		Contact/Email:
SP File Name:	27 optimized.pdn	Design Revision:
Excel File Name:	27 optimized.xlsx	Date: 12/10/2013