

DFM Webinar (Part 1) April 2015

Questions and Comments

The following questions were asked in the chat or question box during the webinar.

Question or comment	Answer or follow up
<p>Is the slide deck available? Is the recording available?</p>	<p>Yes. The slide deck and the webinar recording link are available. Please contact us to obtain it.</p>
<p>[For the PCB board] would it be two inches on all edges, or possibly just two?</p>	<p>This 2-inch requirement is generalization. Not every fabricator requires 2-inches, but some may depending on their tool and capability. Make sure to check with your Fab and Assembly houses before starting to determine their recommended/required margin requirements.</p>
<p>Isn't the IPC clearance for fiducials 2R and not 3R?</p>	<p>This was answered in a detail response online (2R diameter, 1R clearance around the fiducial dot as shown below). Since PCB materials can be somewhat translucent, care should further be taken to have other visible features underneath the fiducial or its clearance on other layers as this could degrade optical recognition accuracy.</p> <div data-bbox="797 705 1312 1094" data-label="Diagram"> <p>The diagram shows a central black circle representing a fiducial dot. A larger white circle represents the required clearance. The diameter of the dot is labeled as 2R. The radius of the clearance area is labeled as R. The total diameter of the clearance area is labeled as 3R. The word 'Clearance' is written above the diagram, and 'Minimum' is written below it. The reference 'IPC-7351-3-11' is in the bottom right corner of the diagram.</p> </div> <p>Figure 3-11 Fiducial Size and Clearance Requirements</p> <p>In older equipment more clearance was required due to more rudimentary optical recognition, and larger clearances are a holdover from those days and at sites where such equipment is still in operation.</p>
<p>Orientation in pick and place file is often useless. Orientation/polarity mark should always be shown in silk or in assembly drawings.</p>	<p>The IPC has standards for orientation and polarity. These are followed by Altium Designer's IPC Footprint Wizard, so you could use it (or at least take your lead from it). It is strongly recommended the appropriate IPC specifications be obtained and followed instead of relying on pin 1 markings on the silkscreen. Notwithstanding, pin 1 indications are very useful in debugging and also increase the chances that if a component gets built with improper rotation it would get identified at assembly time.</p>
<p>A lot of my clients lose the original design knowledge and need to re-engineer their own products, so hiding information only causes more problems</p>	<p>Scraps of paper and files in someone's folder invariably get lost over time. The schematic is often the only detailed design document which reliably remains over time. It therefore becomes the key file documenting the design. For this reason it is strongly recommended that design rationale, key calculations and other engineering explanations be included in the schematic in contrast to only using it as a means to define a net-list. By so doing another engineer can come along later and rapidly understand why the circuitry is the way it is and the tradeoffs which pushed it in that direction.</p>
<p>Can blind and buried vias be used by through hole components? So their leads go through the entire board but is only electrically connected as you're showing?</p>	<p>The answer is generally no because blind or buried hole ranges are peculiar to boards and the stack-up not generally or universally known at the time the footprint is made. Through-holes are only drilled after the entire stack is laminated and at that time there is no way to only plate part of the hole. Consider back-drilling. Alternatively consider SMD devices and use vias at PCB layout time to only hit specific blind or buried layer ranges.</p>



<p>If the trace width is called out as 7mil, is that the width of the etch resist or the width of the trace after etching?</p>	<p>Ideally it would be the width all the way from the resist to the dielectric layer. The exact shapes of undercuts and/or overcuts depend on the fabricator's processes. If you need to know that precisely you should definitely check with them. Regarding impedance control, fabricators have typically calibrated their processes to get specific impedances with specific source widths and spacings, so you should work with them to know what width and spacing you should make your artwork so that it will come out correctly in their standardized processes. You should also put requirements in the fabrication notes for them to adjust the specific width traces to attain the required characteristic impedance within specified tolerances. You can also ask them to include impedance test coupons on the panel and require test results from them on each panel as proof of compliance.</p>
<p>What is the purpose of a finish such as a dry nitrogen box? What happens if you don't use one?</p>	<p>In a nutshell a positively pressurized dry nitrogen box keeps the board very dry (too much moisture can ruin boards in assembly) and prevents oxidation which occurs in the presence of oxygen and moisture over time (required for solderability).</p>
<p>Are you aware if there is an industry standard for SMT component placement accuracy relative to pads?</p>	<p>It wouldn't be surprising if there were, but I have never run across it. Notwithstanding, assembly houses are aware of their placement accuracies and can let you know what it is. Remember, for SMD pads, the IPC recommendations make the pads a specific amount larger, and the intent is that the component "floats" in the molten solder paste and auto-centers due to significant surface tension. Of course, this only works if the SMD part is not fixed in position but allowed to "float". It also requires the symmetry of the pads on the part and footprint.</p>
<p>Lead-free HASL may have a different alloy than the solder pot of the wave so it can leach and contaminate the solder pot.</p>	
<p>For the annular rings, should you be adding 4 mils to the radius or diameter</p>	<p>For the annular rings, you should be adding 4 mils to the radius. For example a good via might be 10/20mils to provide a 5mil skirt all around. Then a manufacturing tolerance of +/-4mils would still leave 1 mil of copper in the pad for a high reliability class.</p>
<p>Can't do rework with ENIG?</p>	<p>During the presentation, it was mentioned that rework was not possible if ENIG was used. For clarification, the rework CAN be done in assembly; it generally CANNOT be done in fabrication.</p>
<p>Is there an example of a good template for the PCB artwork?</p>	<p>The biggest issue with finding THE perfect template is the fact that no two boards tend to require the same information. In the end, there is still a tendency for customization. In addition, some of that information is generated by automated processes within a company that may not be applicable to another organization (for example, the format of Bill of Material may be the product of a specific PLM configuration.)</p> <p>One recommendation is to take a look at Downstream's Blueprint. If you are looking for a "templated" procedure and format, this tool is best suited for such an arrangement.</p> <p>http://ninedotconnects.com/products</p>