DFM Webinar (Part 2) May 2015

Questions and Comments

The following questions were asked in the chat or question box during the webinar.

Question or comment	Answer or follow up
I missed the Part 1. Is it accessible?	Yes. Please request the webinar recording via our website http://ninedotconnects.com/webinar-request-dfm
Is the slide deck available? Is the recording available?	Yes. Please request the webinar recording via our website http://ninedotconnects.com/webinar-request-dfm-part2
What was the name of that software from the last slide on creating documentation easily?	Blueprint PCB by Downstream Technologies. You can find the 2-minute video here - http://ninedotconnects.com/video-request-blueprint-pcb
What is the full meaning if IPC?	Believe it or not, this is not a simply straightforward question. The organization was originally titled *The Institute for Printed Circuits* when it was founded in 1957, thus the IPC acronym. It was later changed to *The Institute for Interconnecting and Packaging Electronics*. In 1999, they changed the name again to the *Association Connecting Electronics Industries*. This was to reflect that they were more than just an organization dedicated to PCBs and their manufacturing. However, they kept the IPC logo. http://www.ipc.org/ContentPage.aspx?pageid=IPCs-Name
I don't see the how this information has anything to do with DFM. This is more like design engineering 101. I thought this webinar was DFM in regards to the schematic and PCB?	We wish that to be the case; unfortunately, that is far from the truth. The concepts and principals of DFM are generally simple practices; however, the manufacturing process is not taught to engineers. In fact, PCB design is not taught to engineers. Electrical engineers are taught circuit theory and mechanical engineers are taught mechanical theory (ie, stresses, thermal, structures, etc.). As a result, what may seem simple and logical in DFM does not register with an engineer who does not know the manufacturing process. Not to beat up on academia; however, they seem to be oblivious to the changes in the industry. As a result, we graduate engineers who are book smart, but are not taught the practicalities of manufacturing. 'DFM' can be interpreted as in "how do I pass Fab and Assy requirements onto my CM"? But the concept of DFM really starts earlier in the design project. There are more specifics related to Fab and Assembly as the design progresses, but often when one gets there, they have proverbially “painted themselves into a corner” since they neglected key DFM considerations up front, such as (but certainly not limited to): • There are no defined requirements to meet • No test strategy driven by requirements • No thought as to how it will be assembled • No consideration given to testability • Layouts which do not allow the assembly machines to do their job • Processes which are not within the scope of the fab or assembly

If I inherit a schematic whit by-passed hierarchy, how do I turn it off?	That depends on the tool you're using. If you're using Altium there are several options under the Project » Project Options. But in general it's not as easy as just changing a checkbox. The connectivity methodology should be set up front and consistently implemented all the way through. For example, hierarchy is useful in some instances (such as for repeated circuitry), but a "ports global" philosophy is much simpler and in most cases, is perfectly valid, faster, and cleaner. But if a design already has all sorts of renaming and indirection in a hierarchical design, it will take a while to make the changes to nonhierarchical. It is recommended to understand the various levels of connectivity and use the simplest one which accomplishes the end goal. A true hierarchical drawing would not simply use a big void block at the higher level, but rather a block that gives some indication of what it represents. This topic could use some more clarification and examples in a future presentation.
Do you suggest placing all test points on schematic?	It is recommended to have a good testing strategy defined up-front before schematic generation, and then use the schematic and other tools at hand to guarantee that it gets implemented. It doesn't take long to set up various components which are test-points of various kinds in the libraries, and then pop them onto the schematic where you know they will be needed to meet that strategy. It is unlikely a PCB designer would know intimately what needs to be tested, how, and why. Remember, a “variant” can strip physical test-points off the production versions to save cost without changing the artwork. The most common problem encountered is too few test-points and no good way to test the circuitry that is buried deep in a BGA package. This is most painful in first article checkout, but can also be true for assembly test. If it is thought-out and consistently implemented from the get-go, it is possible to have boards which are completely and easily testable, and the first article can go to production without re-spins.
If vias are small enough, is there still a solder wicking issue?	You cannot fabricate a via (plated through) with a small enough hole that molten solder will not wick into it. The purpose of soldermask is to stick tightly to the copper and “mask” where it is allowed to wick. Hence offending vias are usually “tented” which means the soldermask covers the via. If you have reasons why you can’t cover it or move it so that it doesn’t wick solder, then you can have it plugged and plated-over, but this is a relatively expensive process.
You can use vias for thermal relief if the vias holes are small enough?	No. You cannot fabricate a via (plated through) with a small enough hole that molten solder will not wick into it. If you’re wave soldering it will be fine as the wave will fill it, but this can’t be used with surface mount parts (typically). In contrast, reflow soldering will allow solder paste to wick to all connected copper which is not covered in soldermask. People regularly use vias for thermal (or high current) connections, but any outer layer copper path between them and connected surface mount pads (i.e. having solder paste) must be blocked from each other by soldermask to stop the wicking.