"DFM Stackup Considerations – Part 4" Webinar August 2015

The following questions were asked during the webinar.

Question / Comment	Response
Aren't the inner signal layer traces classified as embedded micro-strips that have additional calculations for impedance per IPC 2141 section 4.2.3? Does the ICD stack-up planner calculate embedded micro-strip impedances?	Yes, There are different equations for micro-strip and strip-line, and within those there are variants on the equations based on particular aspects of the stack-up such as offset, multi-dielectric, etc. It is important to note that the ICD tool shown during the webinar does not use equations. The field solver in the tool predicts the charge on the particles within the substrate and simulates the impedance using a matrix based on the propagation speed through different sections of the substrate. It also should be noted that built up microstrip layers are simulated, including the inhomogeneous dielectrics of prepreg, solder mask and air.
Why does the prepreg and core have to be interleaved? Isn't the pattern fixed?	Typically the core material is fully cured and the prepreg is only partially cured. Under the heat and pressure of lamination the prepreg partially liquefies and thus fills all the microscopic gaps and sticks to the cores and/or copper. It is this gluing action which bonds the entire board together. So yes, the prepreg and cores need to be interleaved. For custom core thicknesses, several thin interleaved layers of cores/prepregs can be used to build up the desired thickness. Regarding the interleaving, you could specify it, but your fabricator will have specific recommendations and it is recommended you discuss it with them if you want to understand their reasons (which are generally based on their processes.)
Can ICD help with microstrip, patch, or other PCB antennas?	To a large degree, no. Antennas are special resonant structures which require copper clearances in and around them which vary by type, frequency, mode, radiation resistance, and a lot of other things. The ICD tool was not developed to be an antenna calculator/simulator. It can likely help in determining a layer stack-up in support of the feed lines to many antennas.
Can I get more introduction on Soldermask and Via plug? Soldermasks and via plugging versus tenting is a very good subject.	We briefly cover soldermask and via-in-pads in our webinar on DFM – Layer Considerations. However, an in-depth discussion would be a great future topic. Thank you for this feedback.

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On the 8 layer example, could the prepreg and cores be swapped? If not, why?	Yes, in general prepregs and cores can be swapped with each other in a stack-up provided they are the same thickness and material. Note that placing the core material on the outer layers tends to be more expensive (dependings on the fabrication process.) In some cases, it may behoove the fabricator to use the core material for the outer layer in cases where the board has very fine pitched SMD pads. This is due to the fact that the core material has already been hardened and will not suffer from surface contour changes during the lamination process, whereas, prepreg will liquefy during the lamination process and ooze around the contours of the etched copper of the mid layers, resulting in contours on the top copper foil. To the naked eye, these will not necessary be present and for most boards a non-issue; however, with very fine pitched SMA components, these troughs and valleys can be problematic to the assembly process.
As a PCB designer, do I need to specify core versus prepreg?	For "typical" run-of-the-mill boards, 1-4 layers, no impedance control, all SMD, and non-digital, probably not. However, when we are talking about digital boards, we have to assume that it is high speed, even if the clock speed is not considered fast. This is due to the fact that the components are being made on smaller silicon die which in turn, means that their edge rates are faster. Faster edge rates require impedance control to avoid signal integrity issues and this is achieved through the stack up. Therefore, it behooves the PCB designer to consult the fabricator when it comes to the material and its thickness. If you are coming up with the stack up yourself, run the stack-up concept by your preferred fabricator for their approval. They will either accept it or tell you what to change to make it acceptable. They can also tell you what material and dielectric thicknesses they would make it from. Here are a few things to understand and/or ask your fabricator: • Ask your fab shop which materials they stock. If using the ICD tool, the built-in library of materials can assist to get accurate results in terms of thickness, impedances and Trace space/width. • If you need to control this in documentation, ask them to

	send you their recommended stack-up for your board and then document it in your system as appropriate. Note that the ICD Stackup Planner can export a fab drawing containing all the construction info. May sure to add feedback of the fabricator back into the ICD tool. • Make sure the stack-up is symmetrical; choose an even number of copper layers. • The prepreg reduces in thickness as it is fabricated and this makes the signal layers closer to the plane reducing impedance dramatically. • Specify the material you want; if better dielectric constants are necessary, consult the fabricator for availability, price, process issues, and possible pitfalls. Where a stack-up planner can be really useful is on high speed boards with many layers of high density controlled-impedance routing which requires special materials to control dielectric constants, different types of routing to be impedance controlled (single ended, differential, strip-line, micro-strip, offset micro-strip, broadside coupled, various impedances, impedance matching, etc.). It also includes boards with exotic materials to control water absorption, dispersion, attenuation, temperature coefficient of expansion, thermal characteristics, and a raft of other things sometimes required. The ICD includes a huge database of materials and thicknesses to help in choosing. It all depends on what your particular tasks require. If you're making a battery holder for a consumer product, the requirements will be extremely lax. If you're making a high-reliability radar detector for use in military spacecraft, it will be the exact opposite.
How does it "plug in" to Altium? Or is it completely standalone?	The ICD tool is a standalone tool. This was true even when ICD was being sold by Altium. The ICD tool can export the stack up information in a .stackup format and can also insert design rules to Altium. It can also export information in other common formats (ie, .csv, etc.) in addition to exporting to other EDA tools.
Does ICD help identify standard core sizes, or help guide the user to choose standard core sizes?	Yes, it has a database of thousands (+30,000) of core, prepreg, and solder mask sizes. As of the time of this writing, ICD library contains 16,870 materials up to 100GHz
When do you need to consider plane capacitance when designing your stack-up?	Plane capacitance is fairly "high-Q" but small in the overall scheme of things and so usually only comes into play when: 1) You're dealing with ultra-high frequency components (such as bypassing fast rising edges), -OR-

	2) Combining it with other small values (such as trace inductance) to determine an important characteristic such as characteristic impedance or propagation speed. In the ICD tool, this is handled within its 2D BEM field solver for width, spacing, and dielectric constant, so you rarely need to calculate it on its' own. That said, plane-to-plane capacitance can be important if you're trying to isolate the effects between parallel planes (such as one for analog and one for digital). In such a case the best solution is to not overlap them in any area of the board (i.e. have the analog circuits in one area of the board and the digital circuits in another non-overlapping area of the board). Though we did not discuss this in the webinar, one can use planar capacitance to lower the Power Distribution Network (PDN) impedance to about 1GHz. In the ICD tool, the stackup data can be transferred to the PDN Planner for analysis.
In Altium Layer Stack Manager (w/o IDC), I see it provides an impedance calculation. Does native Altium provide for determining impedance of the stackup? Does it provide some of the functionality found in ICD?	First a technical clarification: In a purely technical sense layer stack-ups do not have impedances per-se. However, traces routed with particular widths and spacings to other traces within that geometry will have characteristic impedances. Hence controlling characteristic impedances (and crosstalk, etc.) is a two-step process of first choosing a stackup with geometry capable of generating the characteristic impedances you need using reasonable trace and space widths on pre-chosen layers, and then second choosing and routing trace widths and spacing on those chosen layers to make that happen in the real board. The board stack-up pertains to the first of these two steps. Altium Designer includes equations for the characteristic impedance of the most major types of impedance controlled routing as well as design rules for automated routing by characteristic impedance. However, the equations are based on a 25 year old IPC-317 standard that is now known to contain inaccuracies. This is why ICD created the stack up planner which uses a field solver to provide much more consistently accurate impedance results. Altium does provide the ability to rewrite the equations using their query language; however, we must stress that field solving is far more accurate than equations.

What are the limits on layer numbers?	Altium supports at least 32 copper layers plus at least 16 planes. But we don't know the limit as we have never needed that many. As for the ICD tool, it is capable of an unlimited number of layers. The highest layer count boards are typically large backplanes, but they rarely need anywhere near this many layers if properly designed. Also note that boards with this many layers would be very thick, and as a result would need large diameter vias to keep the length to diameter ratio acceptable for fabrication.
Does ICD identify IPC standard callouts for the various materials? (e.g. "IPC4101/26")	No, not at this time. Though it provides a library for guidance, the selection of materials is based upon the user's determination and fabricator's recommendations.
Is there a generic term for core or prepreg that I can call out in my stackup?	In Altium Designer's Layer Stack Manager the terms "Core" and "Prepreg" are used in the Material column. For the Dielectric Materials and Layer Name columns you can use anything you want.