Nine Dot Connects

Deep Dive – Via
September 23, 2015

Questions & Answers

Via Types		
	Question	**Answer/Comment**
1	Does the Altium package available include all known Via types? Blind Vias? Buried Vias? Thru Vias?	Altium does all 3. In fact, any PCB tool should be capable of provide all 3 types. When it comes to odd vias (like microvias, or vias-in-pads) Altium can do these as well; however, they need to be understood by the designer and noted in the fabrication instructions. The bigger issue to consider is WHEN to use them. All the tools we have seen allow the user to place vias as they see fit; however, the use of blind and buried vias need to be part of the stack up strategy. Otherwise, one can route a board and submit it to fabrication, only to find out that the board cannot be manufactured.
2	Please discuss Vias-in-pad, specifically for thermal dissipation to a copper pad on the bottom of the board.	Via-In-Pad works well to directly couple heat from BGA pads through the board. However, the various pads are connected to a lot of different nets, while there are very few planes which can be used to spread heat across the board. Thus it is really only effective on the BGA pads electrically connected power and ground planes used by the BGA. Using vias between pads to conduct heat is not as effective because there is now a trace it must follow before starting through the board, but these traces are short and in some cases vias can be slightly larger than pads having larger barrels which conduct more efficiently through the board. Plugging holes with silver-filled material also helps, but the process has many steps and hence is expensive.
3	How could vias effect the cost of the PCB? (Too many, too small, filled in, etc)	Every operation adds cost and it can get very high if you're not careful. I've seen bare boards exceed $2000 each when using a lot of specialized processes. However these processes are constantly changing, so you really should get some tentative quotes to decide whether the return on investment is worth it.
4	How prevalent in the industry are the use of blind and/or buried vias?	In inexpensive board they are almost never used due to cost. In high priced high end board they are fairly common. A moderate cost alternative to consider is back-drilling. Another alternative can be done using microvias.
5	What is the typical cost added for introducing blind and/or buried vias?	It varies by fabricators and implementation. It is best for you to contact several fabricators with a board you consider

		"typical" and ask them to estimate it with and without blind, buried, or both. NOTE: it will depend on how many layer ranges you want. The fewer the better.
6	How prevalent in the industry is the use of via in pad technology? <u>Related Question:</u> What is the typical cost added for introducing the use of via in pad technology?	In economical boards – Never. When customers choose to use extremely fine pitch parts, it can get to be pretty much the only option in spite of being quite pricey. As for price, this is a difficult question to answer. There will definitely be a cost due to the number of steps that are added to the process to create vias in pad.
7	For filled vias in pads which is better conductive or not conductive fill and why?	Conductively filled vias improve electrical and thermal conductivity. But its hard to get the fill to go through small diameter holes, especially if they are long. They sometimes have to resort to things like rotary squeegees under a vacuum, etc. This can give rise to trapped bubbles which pop during soldering splattering molten solder from balls. Material which is not conductively filled tends to have these problems much less frequently. If you use it, consider X-Ray microscopic inspection.

Annular Rings		
	Question	**Answer/Comment**
1	Annular ring on an inner layer of a via is (with Altium's default settings) automatically removed during Gerber generation if there is no trace or other connection to that ring/pad on the inner layer. Why is this preferred or not preferred? Copper pours and copper spacing rules will work as if the ring/pad is present, even if it is dropped during Gerber generation. <u>Related Question:</u> What are the advantages/disadvantages to removing internal annular rings on unused layers? On a multilayer PCB, is it preferred to leave the pads on the inner layers, or remove them?	1) Yes, the default in Altium Designer when Gerbers are generated is to remove unused inner layer lands. This can be changed by a checkbox when Gerbers are run or configured within OutJob file. 2) There exist differences of opinion on whether it is better or worse to remove these lands. Some failures early in the use of multilayer boards revealed delamination of the plated barrels from the sides of the drilled holes. It was found that keeping these inner layer pads helped stabilize the barrels during some flexure and prevented this problem. It was also found that when the inner layer pads were removed, PCB designers erroneously thought they could route traces closer to the hole on inner layers. You can remove them, but you must still route as if they were still there. Hence when possible, it's best to leave them there when routing and only remove them as Gerbers are being generated. Recent reports on current fabrication practices suggests

		reliability may be higher with the unused inner layer lands removed. Unless your particular PCB tool/version is configured to not let you use the apparent space, the second problem may still exist in your tool/version. Apparently Altium has attempted to address this automatically in recent versions after receiving feedback from users.
2	Layout engineers may want to change to Top-Mid-Bot or Full-Stack defined vias to minimize the swiss-cheese effect of thermal vias passing through unconnected polygon-pours on inner layers because polygon-pours are often used to create the effect of 'split-plane' layers, but their clearance is based on the annular ring rather than the finished hole size.	If a thermal via array of one net does not connect to a plane of some other net on some internal plane layer, discontinuous interstitial swiss cheese copper can be generated. This can be removed by changing clearances on these layers, using rooms, adjusting minimum pour areas, specifying removal of unconnected copper, or selectively adding keepout polygons or fills. It is typically fallacious to eliminate lands on layers with planes or pours to allow the planes or pours to coalesce, as most of any typically land is still required to accommodate manufacturing tolerances on the hole locations and diameters. Trying to use this space often results in bad boards. From a signal integrity standpoint, such changes to the layer connectivity is not a good practice midway through any design, especially in high speed design. The layer connectivity needs to be thought out at the beginning when the stack up is being considered. Changing these midstream may change impedances, crosstalk, time-of-flight, or impact the rest of the stack up adversely.

Hole Size		
	Question	**Answer/Comment**
1	Plane layers calculate clearance based on the finished hole size for vias, but the actual drill size clearance may change depending on the typical practices of the PCB fab house as they adjust the drill size larger according to the required via plating thickness. Is there some setting in Altium to set the via plating thickness to cause Altium to parametrically adjust?	You bring up a good point; however, as far as we know, Altium Designer does not have the ability to adjust the plating thickness **parametrically**. However, parameters as text strings can be predefined and displayed in notes in the output files you provide to the fabricator. Remember: 1) You are in control of the specifications you send to your fabricator and they should not be changing things in violation of the restrictions you specify without your review and approval. If they are, you should find another fabricator. 2) If you are not including significant and sufficient specifications in your design outputs (i.e., full fab drawing with notes and specifications on all aspects) and instead are relying on the fabricator to "do what they think best," then you not in control of your design process.

		3) A recommendation is to set up a template project with a full set of specifications and output generator configurations in it. Always start with and use this, making only corrections or loosening specific requirements if you know it will be acceptable. 4) Make sure receiving inspection (and that may be you if you are in a small company) verifies the board to the Fab Drawing, and make sure the supply chain is vetted to assure they are always following the drawings unless otherwise directed in writing.
2	Some manufacturers of components that generate lots of heat – such as white LEDs, are recommending via wall copper plating thicker than the common 25um plating, with 35um being a common recommendation. What DFM rules should be observed for those kinds of changes? Related Questions: How do I determine optimum via size for heat transfer? How does one size the pad needed for a via based on the drilled or finished hole size. Specifically if the drilled or finished hole size is 0.015", how big should the pad be to accommodate the via? Does this change for a Class 1, 2, or 3 board?	The process limits of different fabricators vary, so when pushing the limits, you need discuss it with the fabricator(s) that you are considering. Thicker plating takes longer to plate, costs more in terms of machine time and materials, and reduces the finished hole diameter. A Length to Diameter (L/D) ratio of 8:1 is preferred, although most board houses can push it to 10:1 or 12:1. The problem is that as they push the ratio higher, it becomes increasingly more difficult to control the plating thickness at the centers of the holes' length within the stack up. This thinning is not desirable if you're trying to conduct maximum heat through this copper, so you have to limit the L/D ratio. Note that the lower the thermal resistance, the shorter the distance the heat flows, so determine how thin the PCB can be to meet other constraints. You may wish to seek reputable PCB fabricators capable of higher end work to ask them at what L/D ratio is necessary to hold the finished barrel thickness to ±10% of what has been called out by your specification. In addition, you will need to ask how thick they can practically make the copper in the hole at that L/D. Also ask them the minimum drilled hole diameter they can drill and plate in this fashion, and what a reliable minimum spacing between such drilled holes would be. If they can't answer such questions on their processes, then don't use them.
3	When plating, how much typically gets into a via, compared to what is deposited on the surface traces of the PCB?	Near the entrance to the hole it's essentially the same. As you move toward the center of holes it typically gets less. That's one of the reasons for the Length-to-Diameter ratio that the fabricators limit. NOTE: There are specialty houses out there who (for a large fee) will plate holes up to 25:1 very well and sometimes up to 40:1. Don't plan on using them for regular products due to the cost.

4	Is there a typical size hole that is used for a via?	Historically, the board thickness has been 1/16" or 62.5mils. At a length to diameter ratio of 8:1, that makes the smallest normal hole 7.8mils. Thus for Imperial units, the most common small drill diameter for run of the mill holes is 8mils. By the time it's plated with any significant thickness it ends up less than 8:1 L/D ratio, so it is recommended that one sticks with 10-mil drilled holes for the smallest vias. These can be plated with 1 mil thickness in the barrels and still come out 8mil (8:1 L/D).
5	How much bigger than the hole should the pad be?	It depends on the purpose of a pad. A pad is typically where the part attaches. There are tolerances associated with both fabricating the pad and placing the part. In general it should be big enough that with worst case manufacture and placement each pad will still be under the component's corresponding leads with sufficient margin to support proper solder fillets.
6	24) What is the industry recommended general via size (finished drill hole diameter and annular ring) to transfer your general run-of-the-mill signal from one layer to another layer without incurring additional PCB fabrication costs?	Rule #1: L/D ratio less than 8:1 Rule #2: Ask your fabricator what their standard drill sizes are. They may to metric, or imperial, or both. Rule #3: Determine preferred finished hole sizes by subtracting twice the plating thickness from the standard drill sizes. This makes it easy for the fabricator.
7	When showing a drill chart on a PCB drawing, is that the finished hole size, or the size of the drilled hole that is typically specified? How does the size of the drilled hole relate to the size of the finished hole? Does a 0.012" drilled via hole end up at 0.012" finished, or is it more like 0.010" or some other number?	Finished hole size is after plating. The necessary drilled hole size must be larger than that by twice the plating thickness in the holes. It is more common to specify the finished hole size on documentation, but as long as you're very clear they will probably work with you on it.
8	What is an appropriate barrel plating thickness for **<u>high reliability</u>** vias?	As thick as practical. The reliability of vias improves when: 1) The thickness of the copper plating is increased. 2) The coefficient of thermal expansion of the copper matches that of the dielectric 3) The length of the barrel is decreased (i.e. a thinner PCB) 4) The thickness diameter of the barrel is increased (i.e. a larger hole)

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		Points 3 and 4 together equate to decreasing the Length to Diameter ratio of the hole.

Component		
	Question	**Answer/Comment**
1	How does one handle 0.5 mm pitch BGAs when the rest of the board does not have such a component that demands strategies that require a higher cost to fabricate? For an embedded system there might be one 0.5 mm pitch BGA on a PCB but supporting it drives PCB manufacturing cost for the whole board. Choices are, for example, a high aspect ratio for top to bottom vias, adding blind vias that are only useful or necessary in one part of the board, using filled vias in the BGA pad.	Unfortunately, that's the cost of using such small devices. One should always question the need for a fine pitch part before committing to it. Better still, is the component available in a bigger package? The industry is constantly moving toward smaller and smaller devices because that's what customers are said to be demanding. Do we at Dot Connects agree that this is always the case? Absolutely not. Usually the size decision is arbitrary and size requirement is given way too much priority for perceived aesthetic reasons. In going back to the question, one recommendation is to put it on a separate tiny board which merely fans it out to a coarser spacing. It would seem more economically viable to only subject the tiny adapter board to the high costs of ultra-specialized PCB techniques and allow the rest of the board to be designed with relaxed requirements and economical processes.
2	For Thru-hole components, how much larger than the lead should the hole be? Is it better to do it by percentage or fixed size.	If the hole were the size of the component lead it would be hard to get it in the hole and solder may not wick between tightly pressed surfaces, leaving room for corrosion. If the hole were too big and the lead were to one side of the hole, the solder would fall out (or jostle out). Of course this depends on the type of solder. There are lot's or rules of thumb, but here are a few typical ones: • 7 to 15 mils over in diameter is a good choice for round wires in round holes when used with eutectic (63/37% Sn/Pb) solder because it has a lot of surface tension. • 5 to 10 mils over in diameter is a good choice for round wires in round holes when used with Pb-Free solder because it has less surface tension. • 2 to 4 mils over the diagonal dimension for square pins in round holes.

		• As small as can reliably fit worst-case dimensions of a thin rectangular lead in a round hole. • 7 to 15 mils in each direction over the worst-case dimensions of a rectangular lead in an rounded rectangular hole. In each case it is imperative to make sure the leads with their individual and collective dimensions and tolerances will fit with relatively low effort into the pleated through holes in the board without deforming them or the plating in the holes. Consider IPC 2221 for more information.
3	Many power packages today have a solder-pad underneath the part to help with cooling. What size vias should be used (namely finished drill size to spec) in these pads? Too large will allow the solder to drain out and may cause too little solder to be present – or would surface tension keep the necessary amount of solder from draining out? For an example take a look at the LTC3124 datasheet, page 15, Figure 6 Example PCB Layout. Notice the large number of vias under the part.	Unfortunately, many datasheets call out thermal pads without giving proper recommendation or thought to the assembly issues. Not to beat up on LT, however, the LTC3124 is a perfect example of this vagueness. *"It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the IC and into a copper plane with as much area as possible."* One way to handle this is via in pad. However, if you have some real estate available under chip, you can have vias that make contact around the periphery of the thermal pad with the instruction of tenting those pads (and holes.) This allows the pad to connect to the plane thermally without the solder of thermal pad wicking into the via holes.
4	Is there any reason to provide thermal relief on vias that are not the pads of a through hole component?	Generally speaking, no. The thermal reliefs are used to slow the thermal flow to allow the solder to heat up to the desired temperature. If a component is not going to be soldered to the via, then there little point in adding the thermal reliefs.
5	How to use vias for thermal release? How many vias should be put around the components?	Thermal paths can get complex, but the simplified version is: 1) How many total Watts of heat need to be dissipated from a heat source, 2) What is the highest design temperature is you can tolerate at the heat source, 3) What the maximum temperature of the cold sink will be when dumping that amount of heat into it worst case, 4) From this you calculate the minimum acceptable thermal resistance to conduct this heat from from source to sink. 5) Then choose the thermal via shape you can make based on your plating thickness. 6) Calculate its thermal resistance. 7) From 6 calculate how many thermal vias would be needed in

		parallel to meet 4). This is a simplification. You also need to take into account other thermal resistances on the board. And always add more vias than this minimum.

Board Level Considerations		
	Question	**Answer/Comment**
1	Vias on high paths: Making a trace wider makes an obvious change in resistance. Making via diameters wider means more copper because the cylinder diameter is bigger but it also means more void in the middle. Do larger diameter vias have thicker copper better because of better liquid flow through them during plating? Are more small vias better than a few larger vias? Can you provide rules of thumb for making this decision?	As a technicality, making the trace wider results in a change in the impedance, which is defined as both the resistance and reactance. This is important to understand because the reactance is very much influenced by the frequency of the capacitive and inductive effects on the trace. That said, plating thickness decreases in nooks and crannies such as in the center of very long vias, but for reasonable L/D ratios, it can be considered constant. If the plating thickness is constant, the cross sectional area of copper in a via barrel goes down LINEARLY with its radius. At the same time, the number of vias you can put in an area goes up like the square of the area allocated to them. Thus the resistance is minimized by using the smallest vias possible, while packing them as tight as possible. For a given board, first determine the thinnest board you can make, as shorter barrels conduct heat a shorter length reducing the thermal resistance. Then ask your fabricator how small a diameter via can be reliably plated for your thickness of board. Also ask them what would be the closest reliable center to center spacing for such holes. Armed with this, set up a hexagonal array of vias matching this via spacing and diameter. (Hexagonal packing is tighter than rectangular packing.) Note that in some cases solid copper rivets can be soldered into boards to get higher heat conduction, but this a very rare practice and hence not recommended.
2	Ground/power plane stitching vias: what density is best? How to balance connecting planes with the same signal, e.g., GND, with putting more holes in other planes such as power.	An Ultra-Brief Answer: First make your board with a big enough margin you will have room to add vias as needed. Otherwise you will already have shot yourself in the proverbial foot!

		Second, determine the shortest wavelengths (highest frequencies) of any significant harmonics you'll be trying to bypass. (This is usually 10 to 100 times the fastest edge rates used on the board, but is affected by many variables too big to thoroughly discuss here.) Third, try to keep vias sprinkled around randomly, typically no more than one quarter the wavelength you determined before. Fourth, you can increase the spacing after you get several wavelengths away from the signals in question. Note that the above is intended to be a very abbreviated approach to a very complex problem and as such there will be those who take exception, arguing for a more rigorous approach all the way up to rigorous mathematical analysis and full simulation.
3	19) At what frequency should I back drill vias to prevent reflections?	It's a little bit subjective and there are lots of ways of approaching it. Everyone has their PCB Guru so pick the one which works for you. One intuitive way of looking at it is: A ¼-wave stub on a transmission line has drastic effects. A stub only 1% that long may be tolerable. So of all the energies you're putting down this trace, what is the highest frequency of any significance? (For digital signals (only) it will be related to the rise and fall times.) Based on the materials and trace configurations of your board, what is the approximate propagation speed? So how far will this highest frequency travel in ¼ of 1% of 1 cycle of this frequency? If your stub is longer than that you probably need to consider trimming it. (Special Note: Different signal types can tolerate more or less distortion of various harmonic content. Analog signals are fairly sensitive to minor distortions. Digital signals are fairly robust to them. One size does not fit all.)
4	How far apart should vias be for stitching around ground planes? Is it frequency dependent?	Let's flip this question "on its head" for a moment: What size holes can you have in a bag of assorted marbles to keep them from falling out? Since vias "staple" the planes together they constitute low impedance points where currents can flow but voltages are zero. A half-wave can fit thorough between the vias. So again, of all the energies you have in this vicinity, what is the highest frequency of any significance? (For digital signals (only) it will be related to the rise and fall times.) Based on the materials

		and trace configurations of your board, what is the approximate propagation speed? So how far will this highest frequency travel in ½ a cycle of this frequency? If your vias are this far apart or further than that you probably need to consider adding more. Also, note: It is not generally good practice to space all the vias evenly. This could create a high gain aperture antenna. Random spacing eliminates the high gain.
5	Can you discuss the placement of vias near electrically noisy components? I have seen recommendations for X2Y capacitors, various pins on controller chips, etc.	Johansen's X2Y "chip" capacitors are somewhat lower inductance but physically bigger. They typically perform slightly better in the few-hundred MHz region **provided** they fit well within the particular ball grid array pattern. A key thing to remember is that at these frequencies, inductance is begins to dominate. Reducing inductance is key to reducing noise in this frequency range. Also remember that via inductance goes down with increasing via diameter, and in addition to paralleling more vias. If you wish to get mathematical, here's the equation: $L=5.08h[\ln(4h/d)+1]$
6	What effect to vias have on radiated emissions in different types of situations? For example, in the case of a DC-DC (or AC-DC) converter, what happens when incoming power (B+ line) goes through vias? What happens when the switch node has vias to other circuit layers to increase heat dissipation? What happens when the main current loops in a converter have to go through vias to other layers to complete the circuit?	Vias have length, as well as capacitance and inductance which store energy with changes in voltage and current, respectively, and thus could exhibit resonance if not properly terminated on each end. If they were perfectly matched to a trace flowing in and a trace flowing out they would act like part of a transmission line and apart from their time delay be fairly well behaved. With switching power converters the EMI problem usually arises with respect to switch two different but related things: 1) a switching **node** which has very fast **voltage** rise and fall times, and 2) a switching **loop** which has very fast **current** rise and fall times. The voltage node couples by capacitance injecting currents in other nets. The current loop couples by inductance inducing currents in other loops. The key is to keep the switching node very small and far away from other nodes to reduce capacitance, and to keep the switching loop very small and far away from other loops to reduce mutual inductance.

		A via spreads the switching voltage-node and/or current-loop onto other layers, increasing its exposure and breaching any plane it passes through. Which lines carry switching depends on topology. A Boost converter has fairly constant current on the input but switching current on the output. A Buck topology has fairly constant current on the output but switching current on the input. A via in the constant current side is fairly benign, but a via in the switching side should be carefully isolated, routed, and matched. Elimination altogether is preferable.
7	How does velocity of propagation change in the via vs. in a straight trace?	Speed of propagation slows down in the presence of higher dielectric constant. The Velocity Factor equals the reciprocal of the square root of the dielectric constant. When running along the surface of the board, part of the electric field is in the board material, and part of it is above the board in the air. Thus the effective dielectric constant is less than that of the board material. This makes the velocity factor closer to unity and the speed closer to that of light. When running through the board the electric field lies almost completely in the dielectric material. Thus the effective dielectric constant is higher and equal to that of the PCB material. This makes the velocity factor lower and thus the speed slower.
8	Differential via. How do you reduce the impact in signal quality for high-speed signal? What's the proper rule to apply on high speed differential vias?	This is a big topic, so I won't go into all the reasons, ramifications, and options. However, suffice it to say that 1) Most differential traces are loosely coupled and can go apart and come back together with little effect provided the time of flight for each is very close to equal. 2) Coupling is typically primarily to ground instead of the other trace in the pair so that when they do go apart the characteristic doesn't change that radically 3) The return ground current path needs to remain contiguous and short 4) Adjacent trace coupling doesn't become significant until the length of coupled a parallel run approaches a quarter wavelength. Since the board is electrically thin and assuming ground path return vias are to be provided along with the layer-change signal vias, this can be done. However, it would still be best if

		the vias were also impedance controlled and kept very short.
9	Is there a minimum space between vias? Example, if I want to drop several vias to conduct heat to the other side of the board, how close can I space them?	It depends on the nets and tolerances. In general the via to via land spacing needs to be large enough to properly expose and etch the gaps such that they support adequate electrical clearances for voltage isolation, noise immunity, fabrication tolerances, annular rings, hole-to-hole spacing, etc. There are specialty houses which can do very close spacings but only for very high prices.
10	Should vias be used on the GND panel? Or around the board?	All thermal paths ultimately terminate to the environment. You really need to trace the thermal path out through whatever things are in the heat's path to infinity. 1) For example: If you know you have a known volumetric flow of cold air at a maximum temperature from an external source to use, you should determine how hot that air would get carrying away the heat you're generating. 2) The same could be done for a known volumetric flow of cold water, or radiated into the icy blackness of space. Thermal Vias are only one part of the chain of parts which carry the heat away through your known path. Vias are designed to carry heat through a board from layer to layer. Vias do not eliminate any heat. If you have a component generating a lot of heat on one side of a PCB, vias can be used to carry it to the other side or internal planes. If you have a whole PCB which is getting hot, vias around the perimeter could transfer it from planes in the board to, say, a ledge in a metal housing upon which the lip of the PCB rests and is clamped.
11	Are there formulas to calculate ampacity and thermal resistance for vias?	Since the thermal resistance of copper is far less than the thermal resistance of the dielectric, thermal resistance of a via reduces to, in essence, the thermal resistance of the barrel of the via. The portion in the pads should be included in calculations getting to the barrel. It goes up linearly as the length of the barrel increases, and down linearly with increasing cross sectional area of the copper in the via barrel. Ignoring thermal resistance in the lands: $R = \rho \frac{\pi}{4} (D_{Drill}^2 - D_{Hole}^2) Length$ $R = \rho \frac{\pi}{4} (D_{Drill}^2 - \left(D_{Drill} - 2T_{Plating} \right)^2) Length$

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		where ρ is either the thermal or electrical resistivity in the appropriate units. This is true for either the thermal resistance or the electrical resistance.

Solder Mask / Solder Paste		
	Question	**Answer/Comment**
1	Not purely vias, but a use for vias are Castellated pads. I have started using them on a board but did not find much information/guide lines/rules for them.	By "Castellated pads" I assume you are referring to components like Leadless Chip Carriers (LCCs) which have plated cylindrical contact areas running up the side of the package. In general, these need sufficient area on each pad's pastemask opening to provide the right amount of solder to form fillets of the proper radii for proper component centering by surface tension of the molten solder. It also needs to be primarily outside the component body as the contact is vertically tall leading to surface tension pulling more down and out rather than a more traditional bottom sided contact or gullwing foot which are fairly symmetrically surrounded by their pad. In order to start the wetting in spite of slight misregistrations, a small portion of the pads are typically narrow and run slightly underneath the component body. The recommended footprint shape and pastemask pattern depend on the specifics of the manufacturer's actual implementation and so it is strongly recommended you follow the manufacturer's documentation for specifics. In this case, you may want to discuss this with your assembler.
2	I've been told that putting solder mask over both ends of a via is bad practice because moisture, contaminants get trapped in the via and can expand with environmental changes and crack the solder mask off the board. What are your thoughts on this? Related Questions:	Liquid Photo-Imageable (LPI) solder mask will not reliably "tent" every via. Unless a via is reliably tented on **<u>BOTH</u>** sides it can trap residues and not be properly cleanable. Open vias are cleanable. Hence open vias are much preferable to partially tented ones. Dry-film solder mask can reliably tent a via. Therefore, if you must tent, it would be preferable to use dry film solder mask and make sure either both or neither sides are tented for each via.

<table>
<tr><td></td><td>Is there a good reason to tent or not to tent vias with solder mask on one or both sides of the board?

I would be interested in hearing impact / recommendations surrounding via “tenting”, whether on one side, neither side, or both. Especially as it pertains to solderability of components like BGAs.

I would be interested in hearing impact / recommendations surrounding via “tenting”, whether on one side, neither side, or both. Especially as it pertains to solderability of components like BGAs.</td><td>NOTE: Plugging is also an option to prevent contamination. with a properly plugged via there is no place for contamination, and LPI is much less likely to not cover it. So plugging before tenting is also an option.

Unless you plug a via you should not tent just one side or the other. if you are using LPI (Liquid Photo-Imageable) solder mask do not tent both sides unless the via is plugged as it is not sufficiently reliable. You can tent both sides if you are using dry film type solder mask. If you use vias in pads they should be plugged and plated-over on the top, but obviously not tented over as they form the pad. If traces connect to BGA pads on the top, they every pad should be surrounded with solder mask to prevent solder wicking.</td></tr>
<tr><td>3</td><td>When should I fill vias with solder?
Does that help for heat transfer or for additional current carrying capability?</td><td>It always helps some, but the smaller the via the less it helps with heat. For example an 8mil hole with 1 mil plating is about 44% copper. A 20mil hole with the same 1 mil plating is only 19% copper. The electrical and thermal conductivities of solder are significantly less than that of copper:

<table><tr><td>Metal/Alloy</td><td>Electrical</td><td>Thermal</td></tr><tr><td>Copper</td><td>$1.68 \times 10^{-8} \Omega m$</td><td>398W/(m·K)</td></tr><tr><td>PbFree Solder</td><td>$1.65 \times 10^{-7} \Omega m$</td><td>57W/(m·K)</td></tr></table>
Thus is helps very little in small vias, but could help some electrically in large vias.</td></tr>
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