The Test and Prototyping Group

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Here's a scenario that many of us may have encountered some time in our life – You just got home from the local electronics store with a new appliance and the entire family is feverishly anticipating its use. . . only to discover that it does not work! Sure enough, aggravation sets in quickly: lack of immediate use, repacking it right after your son busted the Styrofoam into a jigsaw puzzle, driving it back to the store and ultimately having to make a decision. Do you replace it with the same model suspecting that the entire inventory of that particular model is also defective or spend more time on investigating another brand?

We expect our electronic purchases to work the first time, which is not an unreasonable assumption. A good manufacturer, whether it be refrigerators or silicon fabrication understands customer satisfaction. This concept is no different in the design services offered by Cadence Design Systems. When our customers hand us a design requirement, they expect an operational product. This expectation is the primary job function of the Test and Prototyping group in San Diego, CA.

The Cadence Test and Prototyping Group plays a pivotal part in the evaluation of the silicon designed by both Cadence and the customer. Our responsibilities include, but are certainly not limited to: characterization, debug, production flow, bench testing, loadboard and probe card fixturing, test specification development and test, packaging & manufacturing support. Our group is responsible for three test floors throughout San Diego with over 20 million dollars in equipment at our disposal to verify the end product. Though our capabilities have been primarily in digital test, we have expanded our services to handle mix signal and analog product.

Loadboards? Characterization? Probe cards? Manufacturing? Packaging? At first glance, this does not seem to fit the image of Cadence. However, it does provide additional capabilities and an added value that few other design houses can offer to their customers. Once a design has been placed on silicon, the Test and Prototyping group provides "cradle to grave" support. It should be noted that Cadence is not a silicon manufacturer nor does it own any assembly or fabrication houses. The Test and Prototyping Group supports and out sources its assembly needs to various vendors based on customer, material and volume requirements.

This is a the Credence ATE Duo System. It is capable of testing a device with 512 IOs. The unit is composed of a SPARC station, test head (on the far left) and a bay which houses the logic boards of the systems.

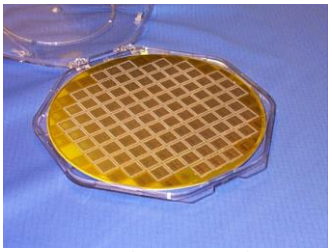
When does the Test and Prototyping group become active in a design project? The group's preference is to be involved when a design project is first being scoped. Based on the design requirements, customer preference and hardware needs, decisions are made to allocate equipment for the task. Though the group uses lab equipment like oscilloscopes, power supplies, curve tracers, and multimeters, the majority of the testing is performed on Automated Test Equipment (ATE). These machines, some the size of a small automobile, are capable of over a million tests per second, which is truly a necessity when handling designs with high pin counts. Additional criteria to determine which ATE will be allocated is based

on other factors including speed of the device, mix signal & analog requirements and the time available on the ATE (which has to be scheduled to accommodate multiple projects.)

The Test and Prototyping group has flexibility and can offer its services at any time. In some instances, the group has provided production support long after the device was introduced to the market. Such is the case with one of our customers that has been producing a line of radio chips for over 20 years. Recently, they outsourced this line to the Cadence Test and Prototyping Group to establish a full production test procedure and to monitor this production flow. In other cases the Test and Prototyping Group has been asked to handle emergencies. In this capacity, the group is able to provide debug services after the initial product fails to operate.

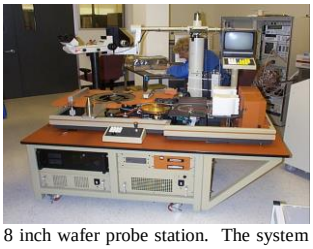
Characterization

When a new device arrives from a fabrication facility, a process referred to as characterization is initiated. This is the evaluation of the chip's performance. The data collected includes information like functionality and yield in addition to measured values like voltage and current draw. The measurements are compared against a specification table, which lists the expected minimum and maximum range within which the device is expected to operate. The specifications are supplied by either customer requirements and/or simulation expectations. In addition, functionality is tested against the vector sets which were initially developed when the device was undergoing design simulation.



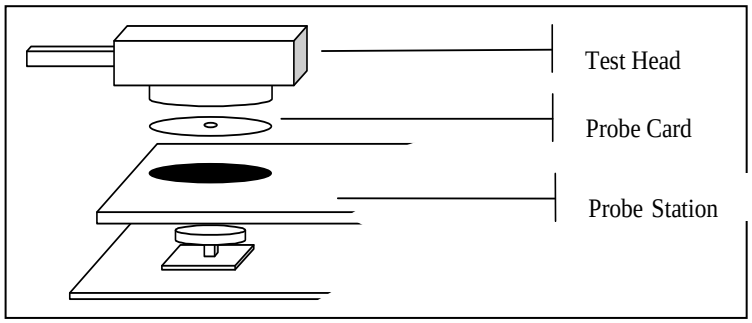
An example of an 8 in. wafer. Each square is an individual die. Through the use of a probe card, prober and ATE, each die can be tested without having to cut the wafer.

An example of a probe card. The strips of gold are contact points to the ATE. The center of the card contains the probe tips which make contact to the bonds pads of the wafer.



8 inch wafer probe station. The system is used to load and manipulate wafers. Most of this activity is performed under a microscope. Bond pads and tungsten tips are extremely difficult to see with the naked eye.

The implementation of characterization is a challenge for both hardware and software. The silicon is shipped in wafer form. This allows the Test and Prototyping Group to verify the die without having to compensate for the package effects. Electrical test is performed through the bond pads on each die of the wafer. The equipment used for this effort include the ATE, probe station and a probe card. The ATE generates the signals to the device and performs the necessary measurements. The probe station is used to manipulate the wafer and to add automation to the process. The probe card is the electrical interface between the tester and the wafer. The probe card is a Printed Circuit Board (PCB) containing Tungsten tips which pierce the bond pads of the die and forms an electrical contact while providing a surface for contact with the tester.

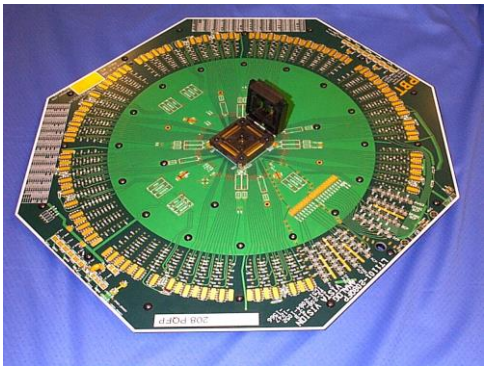


Added caution must be taken during the handling of the wafers. Both the wafers and the probe cards are extremely delicate. Each probe card may cost $10,000 or more to develop and assemble. The

Test and Prototyping Group does encourage designers to re-use existing bond pad layouts (with similar power connections) to save on both the cost and delivery time, which is generally eight weeks.

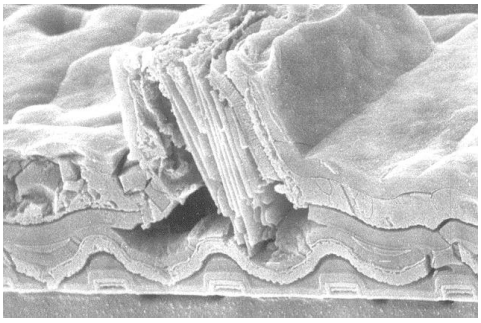
The IDS 10000

Problems with the device may surface during the characterization. The degree of failure ranges from marginal spec failure to zero yielding product. Regardless of the failure it must be investigated. There are many variables which may contribute to the problem: ATE misconfigeration, contact resistance of the probe card, bad wafer fabrication, timing errors on the simulation, to name a few. If the problem is chip related, the group has various options available. One piece of equipment which can be used to debug projects is the Intergrated Diagnostic System (IDS). This is an electron beam microscope that allows the engineer to literally see the activity on the chip.



Loadboard capable of handling a 208 PQFP

The IDS' interface with the ATE is similar to that of a probe station. The ATE generates the signal while the IDS displays the electrical activity to a work station. The interface between the test and the device differs from the probe cards. The wafer is cut into individual die which are then wirebonded and packaged. A PCB similar to a probe card is used to interface the tester to the device which is commonly referred to as a loadboard. A loadboard is a PCB that contains a socket specific to a package type with contacts to interface with the tester.



The Silicon Services Group provides additional resources to pin point the cause of various wafer process failures. In this case, Titanium flaking.

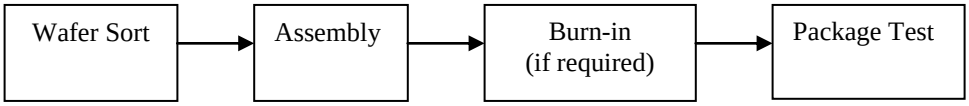
If a wafer process is causing the problem, physical analysis may be required. Test and Prototyping engineers works closely with another group at the Cadence San Diego Facility known as Silicon Services. Silicon Services provides failure analysis using X-ray and chemical etching methods to detect and evaluate defects with the capability to add or remove metal lines to the device . This allows us to recommend corrections to the initial design. (It should be noted that the Silicon Service Group provides a number of other services in addition to failure analysis which included, but is not limited to: reliability, modeling and design rules, all of which are generated from data obtained from device die.)

This characterization process continues until a device performs to specification and is highly dependent upon the number of design changes required and the wait time based on the booking schedule of the fab house being used.

Production and Manufacturing support

The Test and Prototyping Group provides services to ensure that production volume of the design is brought on line as quickly as possible. In some cases, the completion of characterization marks the end of the service contract. Companies that have their own test floors may request the test programs and fixturing used during the characterization process to establish a production flow themselves. If a company does not have this infrastructure, they may opt for the Test and Prototyping Group to handle it for them.

When many individuals hear the word "production," a factory comes to mind with rolling belts and electronic arms welding parts together. Though the factory concept is a good way of visualizing it, the process is more stage oriented, rather than continuous. Generally, the production flow tends to look like:



The first step in this process is wafer sort. This is primarily used to map the wafer for usable die. This stage is similar to the set up used during characterization with the probe station, probe card and ATE. Though the processes of fabrication have greatly improved over the years, not all die on a wafer will be useable. In some cases, the cost to package bad die is greater than the amount of time spent on evaluating the die. However, if yields have been historically high, the volume of product is great, or the package cost are inexpensive, wafer sort make be skipped. This is known as a blind build in which all of the die in a wafer are packaged without being tested.

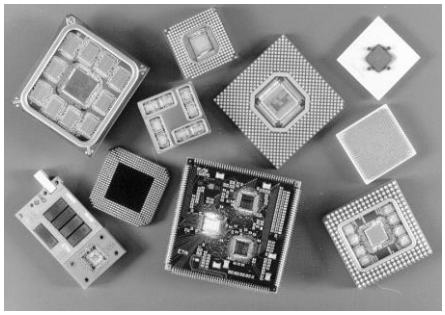
Assembly is the operation in which the wafer is cut into individual die. Each die is placed into package and connected to the package through a series of bond wires. The processes for packaging vary, depending on the packaging materials used.

On method to remove infant mortality of a product is to put it through the process of burn-in. This process is added to the production flow for products which will be used in critical applications or extreme environment conditions such as military, space, medical, or requires a long life expectancy like a mainframe computer. One method to age a device is by applying heat to it. In this case, the device is placed into an oven for a duration of time at a specific temperature. In some cases, an electrical check can be performed on the device during the burn-in process without removing it from its heat duration. In other cases, the failure will be detected upon package test on an ATE.

The final leg of the product's journey is package test. Using an ATE, the package is tested against a similar program used during the wafer sort. Product which fails this test may be analyzed to determine the cause the failure. This information is vital to ensure that the risk of field failures (product which fails in the hands of the customer) are minimal. In a low volume situation, each packaged device may be inserted onto the ATE by hand. However, for lot sizes of 1000 or more, the process of insertion is automated through the use of a device called an autohandler.

The flow described above is not set in stone. There are number of variations and loops can be added or removed depending upon the device. For example, when a multiple chip module is being assembled, a rework loop could be added. In many cases, the number of hours in a burn-in oven may be reduced or even eliminated if data exists to support it. Test times may also be reduced by removing tests which were not critical to capturing failures. However, regardless of the efficiencies added to reduce the production time, the device must be tested prior to it being shipped .

Packaging

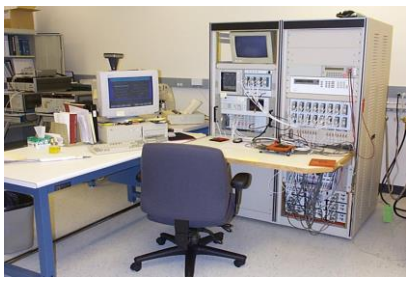


A sample of the various products the group supports, from the simple to the complex and unique.

As the number of gates on a single chip expanded, so did the number of IO signals. Common packages types like the Dual In-Line Pins (DIPS) and Pin Grid Arrays (PGA) which had been used for years are no longer capable of handing the pin count nor the temperatures at which the chip may operate. New technologies are surfacing at a great speed in order to keep the physical size of the chip small while being capable of handling the various temperature and noise stresses.

Packaging is a critical aspect for the Test and Prototyping Group. The package can add a great deal of difficulty to the testability of a product. If contact to the tester is compromised, bogus results may be induced. Like the probe cards, there is a push to reduce cost by re-using existing package types. In fact, in the case of the autohandler, it may cost $30,000 or more to retool the equipment for a specific package type. In an effort to reduce these factors, the group is capable of recommending packages to the customer based on their application needs while keeping cost and testability in mind. Though Cadence is not an assembly house, it must be sensitive to the cost factors in assembly which will escalate if the package requires a great deal of custom, non automated work.

Bench Test



The WGT system allows for precision measurement in addition to preconditioning and automation of measurements

Though the ATE systems handle a great deal of the test necessary to complete a characterization report, there will be instances when the customer requires testing above and beyond the capabilities of the ATE. Test such as ground bounce, capacitance and inductance are generally performed on bench equipment. The Test and Prototyping Group has automated a great deal of these tasks through the use of Lab View and the purchase of the WGT system. When in doubt, we do rely upon multimeters, logic analyzers and oscilloscopes to take the hand measurement.

The Test and Prototyping Group has a great deal of services to provide to both the design centers and the customers of Cadence. The information provided in this introductory article only scratches the surface of the group's capabilities. We hope that with the services discussed and equipment presented, we have not only clarified some of the mystery of the group's function, but have hopefully spurred the imagination of those design groups looking for a angle which makes them stand out above other design companies bidding for a customer contract. In addition, we

hope that this will open an avenue of discussion between us, the software groups and the designers. Future papers regarding specific issues, services, equipment, etc. can be written as the requests and need arises.