

DESIGN RULES SUMMARY

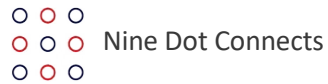
Rule	Category	Real Time	Batch	Auto router	Default On?	Unary Binary	Primary Purpose	Secondary Purpose
ELECTRICAL								
Clearance	Electrical	TRUE	TRUE	Yes	Yes	Binary	MFG - Fabrication	IPC standard
Short-Circuit	Electrical	TRUE	TRUE	Yes	Yes	Binary	NetList Integrity	
Un-Routed Net	Electrical	N/A	TRUE	No	Yes	Unary	NetList Integrity	
Un-Connected Pin	Electrical	TRUE	TRUE	No	No	Unary	NetList Integrity	
Modified Polygon	Electrical	TRUE	TRUE	No	Yes	Unary	MFG - Fabrication	
Creepage Distance	Electrical	FALSE	FALSE	No	No	Binary	High Voltage Integrity	IPC standard
ROUTING								
Width	Routing	TRUE	TRUE	Yes	Yes	Unary	MFG - Fabrication	Signal/Power Integrity
Routing Topology	Routing	N/A	N/A	Yes	Yes	Unary	Tool Handing	
Routing Priority	Routing	N/A	N/A	Yes	Yes	Unary	AutoRouting	
Routing Layers	Routing	TRUE	FALSE	Yes	Yes	Unary	AutoRouting	
Routing Corners	Routing	N/A	N/A	Yes	Yes	Unary	AutoRouting	
Routing Via Style	Routing	TRUE	FALSE	Yes	Yes	Unary	MFG - Fabrication	Signal/Power Integrity
Fanout Control	Routing	N/A	N/A	Yes	Yes	Unary	AutoRouting	
Differential Pairs Routing	Routing	TRUE	FALSE	Yes	Yes	Unary	MFG - Fabrication	Signal Integrity
SMT								
SMD To Corner	SMT	TRUE	TRUE	No	No	Unary	MFG - Fabrication	
SMD To Plane	SMT	TRUE	TRUE	No	No	Unary	MFG - Fabrication	
SMD Neck-Down	SMT	TRUE	TRUE	No	No	Unary	MFG - Fabrication	
SMD Entry	SMT	TRUE	TRUE	Yes	No	Unary	MFG - Fabrication	
MASK								
Solder Mask Expansion	Mask	N/A	N/A	No	Yes	Unary	MFG - Fabrication	High Voltage Isolation
Paste Mask Expansion	Mask	N/A	N/A	No	Yes	Unary	MFG - Assembly	

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PLANE								
Power Plane Connect Style	Plane	N/A	N/A	No	Yes	Unary	Primitive Properties	MFG - Fabrication
Power Plane Clearance	Plane	N/A	N/A	No	Yes	Unary	Primitive Properties	MFG - Fabrication
Polygon Connect Style	Plane	N/A	N/A	No	Yes	Binary	Primitive Properties	MFG - Fabrication
TESTPOINT								
Fabrication Testpoint Style	Testpoint	FALSE	FALSE	Yes	Yes	Unary	MFG - Fabrication	Test and Prototyping
Fabrication Testpoint Usage	Testpoint	FALSE	FALSE	Yes	Yes	Unary	MFG - Fabrication	Test and Prototyping
Assembly Testpoint Style	Testpoint	FALSE	FALSE	Yes	Yes	Unary	MFG - Assembly	Test and Prototyping
Assembly Testpoint Usage	Testpoint	FALSE	FALSE	Yes	Yes	Unary	MFG - Assembly	Test and Prototyping
MANUFACTURING								
Minimum Annular Ring	Manufacturing	FALSE	TRUE	No	No	Unary	MFG - Fabrication	IPC standard
Acute Angle	Manufacturing	FALSE	TRUE	No	No	Unary	MFG - Fabrication	
Hole Size	Manufacturing	FALSE	TRUE	No	Yes	Unary	MFG - Fabrication	IPC standard
Layer Pairs	Manufacturing	FALSE	FALSE	No	Yes	Unary	MFG - Fabrication	
Hole To Hole Clearance	Manufacturing	FALSE	TRUE	No	Yes	Binary	MFG - Fabrication	IPC standard
Minimum Solder Mask Sliver	Manufacturing	FALSE	TRUE	No	Yes	Binary	MFG - Fabrication	
Silk To Solder Mask Clearance	Manufacturing	FALSE	TRUE	No	Yes	Binary	MFG - Fabrication	
Silk To Silk Clearance	Manufacturing	TRUE	TRUE	No	Yes	Binary	MFG - Fabrication	
Net Antennae	Manufacturing	FALSE	TRUE	No	Yes	Unary	NetList Integrity	
Board Outline Clearance	Manufacturing	FALSE	TRUE	Yes	No	Unary	MFG - Fabrication	IPC standard
HIGH SPEED								
Return Path	High Speed	N/A	FALSE	No	No	Unary	Signal Integrity	
Parallel Segment	High Speed	TRUE	TRUE	No	No	Binary	Signal Integrity	
Length	High Speed	TRUE	TRUE	No	No	Unary	Signal Integrity	
Matched Lengths	High Speed	TRUE	TRUE	No	No	Unary	Signal Integrity	
Daisy Chain Stub Length	High Speed	TRUE	TRUE	No	No	Unary	Signal Integrity	
Vias Under SMD	High Speed	TRUE	FALSE	Yes	No	Unary	Signal Integrity	MFG - Fabrication
Maximum Via Count	High Speed	TRUE	TRUE	No	No	Unary	Signal Integrity	MFG - Fabrication Cost
Max Via Stub Length (Back Drilling)	High Speed	FALSE	TRUE	No	No	Unary	Signal Integrity	

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PLACEMENT								
Room Definition	Placement	TRUE	TRUE	No	Yes*	Unary	Primitive Properties	
Component Clearance	Placement	TRUE	FALSE	No	Yes	Binary	MFG - Assembly	
Component Orientations	Placement	N/A	N/A	No	No	Unary	MFG - Assembly	
Permitted Layers	Placement	FALSE	TRUE	No	No	Unary	AutoRouting	
Nets to Ignore	Placement	N/A	N/A	No	No	Unary	NetList Integrity	
Height	Placement	TRUE	TRUE	No	Yes	Unary	MFG - Assembly	
SIGNAL INTEGRITY								
Signal Stimulus	Signal Integrity	FALSE	FALSE	No	No	Unary	Signal Integrity	
Overshoot - Falling Edge	Signal Integrity	FALSE	FALSE	No	No	Unary	Signal Integrity	
Overshoot - Rising Edge	Signal Integrity	FALSE	FALSE	No	No	Unary	Signal Integrity	
Undershoot - Falling Edge	Signal Integrity	FALSE	FALSE	No	No	Unary	Signal Integrity	
Undershoot - Rising Edge	Signal Integrity	FALSE	FALSE	No	No	Unary	Signal Integrity	
Impedance	Signal Integrity	FALSE	FALSE	No	No	Unary	Signal Integrity	
Signal Top Value	Signal Integrity	FALSE	FALSE	No	No	Unary	Signal Integrity	
Signal Base Value	Signal Integrity	FALSE	FALSE	No	No	Unary	Signal Integrity	
Flight Time - Rising Edge	Signal Integrity	FALSE	FALSE	No	No	Unary	Signal Integrity	
Flight Time - Falling Edge	Signal Integrity	FALSE	FALSE	No	No	Unary	Signal Integrity	
Slope - Rising Edge	Signal Integrity	FALSE	FALSE	No	No	Unary	Signal Integrity	
Slope - Falling Edge	Signal Integrity	FALSE	FALSE	No	No	Unary	Signal Integrity	
Supply Nets	Signal Integrity	FALSE	FALSE	No	No	Unary	Signal Integrity	



Notes:

1. This list is based on the DRC rules in Altium Designer 21. Altium will likely continue to add rules in future versions.
2. The "Real Time" and "Batch" columns come from the menu command Tools » Design Rule Check... Under the category of "Rules to Check," all rules are listed, allowing the user to determine when a rule is to be applied.
 - ❖ "Online" allows Altium to check against a rule while edit is being made. For example, when routing a trace, the inability to violate the electrical clearance is due to this rule being "Online."
 - ❖ "Batch" rules are run when the user invokes Tools » Design Rule Check... and presses the "Run Design Rule Check..." button.
 - ❖ Some rules may not have the option for "Online." This is the case for signal integrity rules (run through the Signal Integrity simulation tool) or rules where the rule itself would interfere with editing. For example, if you are routing a net, you would not want to be bothered with an error stating that the net is unrouted.
3. The "Autorouter " column indicates whether the autorouter in Altium makes use of the rule.
4. Many rules are specifically to guide the autorouter, as listed in the Primary purpose column.
5. "Default On?" indicates whether the rule is enabled when one first opens a new .PCBdoc. Many rules are not enabled by default. Make sure the rule makes logical sense to enable before doing so. There is no reason to constrain a design overly.