Routing DDR3 Part 1 of 2 Q & A

Questions / Comments	Answers / Response
What is the best way to determine dielectric constant? How can users properly pick dielectric materials?	The material datasheet is always the best source of information. The iCD tool we presented also has a substantial library over 31,275 of this data. We also encourage you to contact your fabrication house, especially if you are not familiar with the other properties of the materials that may have a substantial impact on the manufacturability or cost of the board.
What value do you use for the propagation delay of vias and why?	Treat the vias as a stripline because the signal conductor is surrounded by substrate.
Why do you call it "skew"? Didn't you just extend the length, which would happen to all lines?	The example was to compare if you route one signal in a group as a microstrip and one as stripline.
This is a question about fly-by routing to two or more memories. With fly-by routing there are stubs from bus to memory pins. When calculating CPU-to-memory #2 signal delays, do we include the stub delays from signal bus to memory #1 pins? The actual CPU to memory #2 flight delay is the bus path. In Altium, do we set up x-signal group from memory #1 pin to memory #2 pin, or from bus-via-near-memory #1 to memory #2 pin?	1. The only delay to calculate is that which is along the propagation path. 2. The stubs are only important if you are calculating timing to Chip 1. Otherwise they do not matter for calculating delays to the other chips. 3. Altium xSignal wizard creates two groups, one to the first chip and one to the second.
Fly-by was mentioned, but it was not actually defined. Can you be more specific about this?	The following is a great article about this topic from Barry Olney, who is not only an expert in high speed design, but is also the creator of the ICD tool: DDR3/4 Fly-by vs. T-topology Routing By Barry Olney Published in PCB Design Magazine Publication Date: April 2016 http://www.iCD.com.au/articles/DDR3-4_Topology_PCBD_Apr2016.pdf

I have to do a DDR4 for the first time, coming up in the near future. How is DDR4 different than DDR3? Are you going to do something for DDR4/5?	At this point, we have not investigated DDR4 in any great length to make definitive comments about the pros and cons between DDR3 and DDR4 (or DDR5 for that matter). For us to be definitive about this matter, we must go through the design process. Given the interest, we will certainly give this request its due consideration.
If traces are impedance controlled, will that not also make the flight times the same if the impedances are the same?	Impedance control is for maintaining an impedance across a layer. In answering your question, the answer is 'no'. Flight times are dependent on the dielectric constant and stackup geometry, not on the impedance. A 40 ohm microstrip and a 40 ohm stripline have the same impedance, but totally different flight times.
Would you recommend iCD as the best software for this type use? My business uses Hyperlynx and am wondering how they compare	Hyperlynx is a higher end tool that requires a significant investment in both time and money whereas iCD is sufficient for DDR3 calculations and other useful functions such as stackup, termination planning, etc. at an affordable price.
Can iCD include via impedance calculation?	It takes the via into consideration since it is a field solver.
Is there a detailed tutorial for using iCD?	No. However, there are numerous examples and videos. Please feel free to contact Nine Dot Connects for more information.
Will DDR calibration, say in LINUX, fix any of this [write leveling]?	Although there might be some control within the OS to calibrate the write leveling, the PCB routing still needs proper management of skews so any external calibration can be effective.
How the rules apply on a two device only T-topology?	Same rules apply regardless of the number of memory chips.
Do we need to be concerned about dog bone via impedance/capacitance in DDR3 designs?	Via impedance is always to be a concern in any high-speed signal transmission.

Can iCD be integrated into Altium?	Though the iCD stack up information can be imported into Altium Designer, the route lengths calculated within iCD will have to be entered into Altium manually.
What was the name of that software, and can it be upgraded with new lists of materials, core & prepreg thicknesses?	It is called iCD and Nine Dot Connects sells and supports it. Check out https://www.ninedotconnects.com/products-iCD-design-integrity The tool provides over 31,275 dielectric materials in a library and they are constantly getting updated.
How does via-fill affect delay, if at all?	A filled via vs. an unfilled via should still have the same delay. Essentially the same concept as a thick vs. thin trace.