Routing DDR3 Part 2 of 2 Q & A

Questions / Comments	Answers / Response
How much of an issue are voids as long as you don't run your diff pair over them? How close can you get?	The recommended clearance between the differential pair and the void is based on the height distance between the diff pair and the plane. The general rule of thumb is that the clearance should be 3 times that height. You could get away with 2X; however, 3X is the safe bet.
How would you go about evaluating the *competence* of a board house with respect to these kinds of high speed routing issues such as fabrication on bias?	A good board house (note: this is not a comprehensive list): 1. Is going to provide you a stack up from the beginning of the PCB layout. This is based on the number of layers you have called out. 2. Is going to provide all of the trace width and space requirements for each layer for each impedance that you have need for. 3. Is going to calculate the impedances using a 3D solving software to ensure that the numbers provided are optimal. 4. Will recommend board materials that they know will be successful. 5. They can recommend glass weaves and board rotation to minimize impacts of the Dk variances.
In the previous session, it was mentioned that power planes could be used for reference planes. Will you talk about how to tie reference planes together in this case? How to "tie" reference planes together when one is power and one is ground? What do you do if your trace goes from a GND reference plane to a V+ reference plane?	Ultimately all power planes and ground planes are tied electrically together through decoupling capacitors. If you strategically place decoupling caps where you want the two planes to be electrically the same at the highest frequencies, you have accomplished making a power plane a contiguous reference for your signal.
How different would this presentation be if it was for DDR4?	DDR4 has its own set of rules and requirements for layout, in some ways similar to DDR3 but in some ways very different. So DDR3 techniques cannot be directly used for DDR4 layout.

Where can we find the pin delay information on an FPGA? How did you determine your pin lengths?	For Xilinx parts, run the Vivado development environment. In the Tcl Console, type: "link_design -part xa7z030fbv484" for example. Use the name of the actual part you are using. Then type "write_csv d:/myfilename" and use the desired file name and location. This will generate a .csv file that will have the pin package delay times.
If I wanted to route 4 DIMMs but only populate 2 now and as an option add the other 2 DIMMs, where would the terminations resistors go? Between DIMM 2 and 3 or at the end of DIMM 4?	The termination resistors always go at the end of the signal path, so in this case at the end of DIMM4. You will have to live with the reflections from the un-terminated stubs for unpopulated DIMMs but the longer stubs to the termination resistors will still be terminated. This is why you populate the slots closest to the controller first.
You mentioned using the dielectric constant to convert time delay in the chip to lengths, where do you get the dielectric constant to use?	The dielectric constant is provided in the material datasheet. However, we do not recommend that you simply select a material solely based on the dielectric. This is a discussion that must be had with the fabricator to ensure that they can use it. Example, there is one particular material has a very low dielectric rating; however, it has such an expansion that using it on more than 2 layers will result in uncontrollable layer and registration alignments.
Wouldn't the width of the serpentine matter also i.e. more chance for coupling? The follow up question: 'Didn't mean the trace width, but rather the width of the meander'	As the width increases, more of the E-field will be under the trace and not part of the fringe. Less fringe means less coupling. So, you are correct. However, most traces are designed for a specific trace width to create a fixed Zo Impedance) so now the gap width is the dominant factor. As for the follow up question, the width between one line to another (even to itself in a serpentine) can cause coupling. If you want to remove any change of coupling, refer to the rule of thumb regarding clearances: The clearance between 2 signals is based on the height distance between the aggressor signal and the plane. The general rule of thumb is that the clearance should be 3 times that height. You could get away with 2X; however, 3X is the safe bet.

Is there a difference between accordion vs. trombone serpentine	Unless you are doing gigabit design, the shape of the serpentine will not matter.
Do you have any examples of using the Signal Integrity rules in Altium to check for timing delays?	Though it could be done, it is not without some effort and issue. The S.I. rules only work on IBIS files. Therefore, you will have to obtain the IBIS for each component and then make sure that the model is set correctly for each pin. The issue with Altium S.I. is that it only can handle classic 'signal to plane' calculations for cross talk and delay. It cannot calculate the effects of copper pours. This is due to the fact that the S.I. tool in Altium is not a field solver which can take into account any shaped copper. Check out the video on SI in Altium Designer - https://www.ninedotconnects.com/video-signal-integrity
Can you talk to the tradeoffs of fly by vs T-topography?	Fly-by is intended to make the routing easier when using more than two devices (although it also works with just two.) T-branch requires balancing more signals, and also makes impedance control more difficult. For DDR3, you are required to use fly-by for more than 2 devices but can use T-branch for two if you desire.
In the layout example, it was mentioned that package delays for the controller were converted to lengths to use in Altium. How is that conversion made without knowing the equivalent dielectric constant in the controller package?	Since we are looking for the equivalent trace length for the existing PCB only the dielectric constant for the PCB is needed. Using this Dk and the given pin package delay time, solve the propagation equation for trace length and use that as the pin package length.