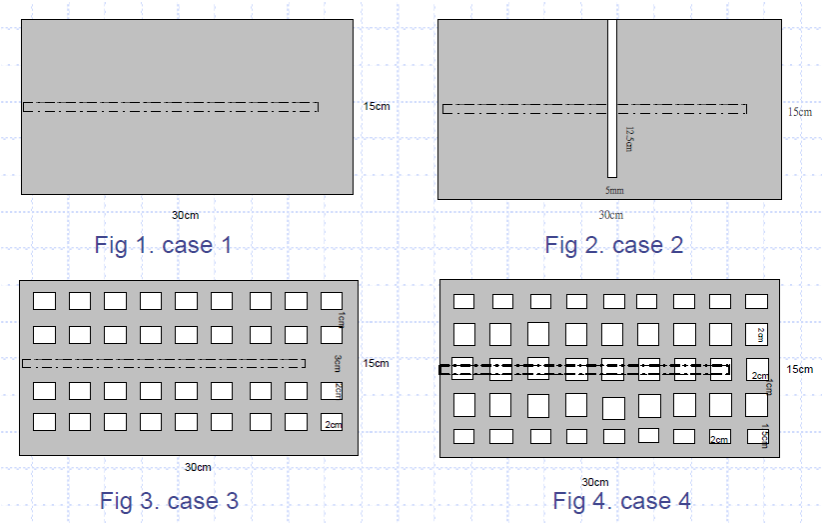
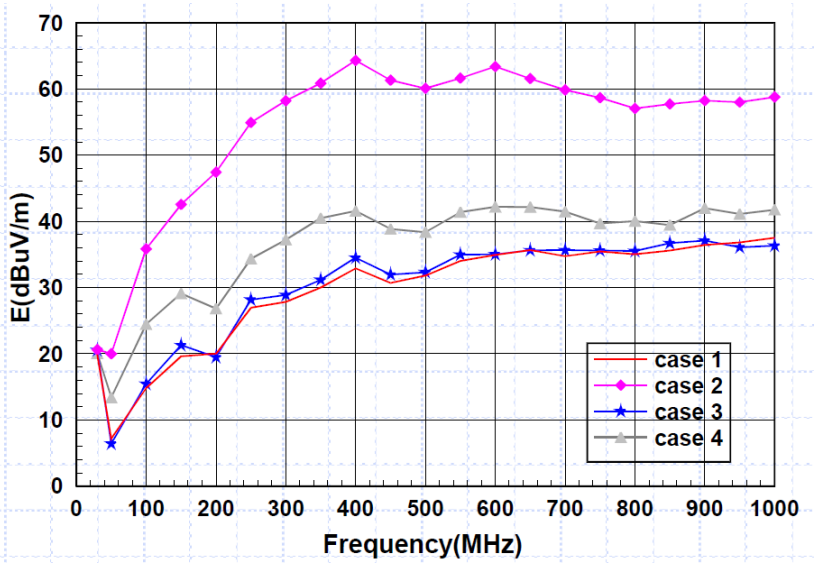
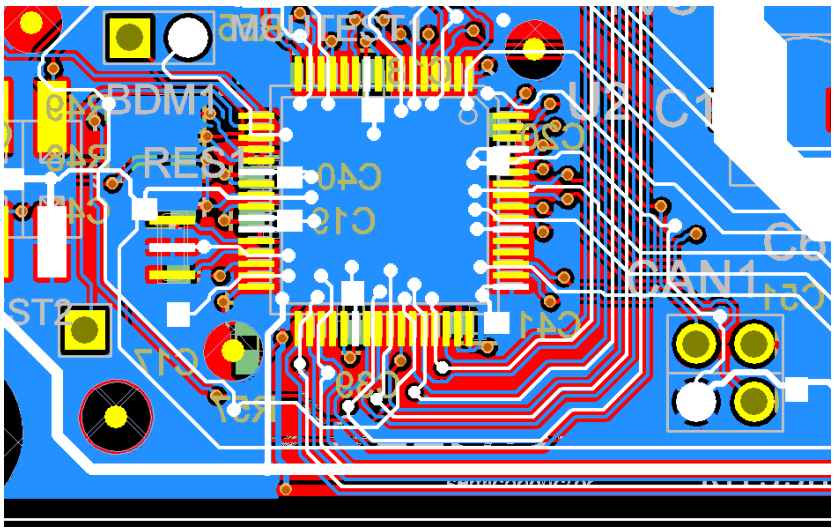
What Drive a HS Signal – Voltage or Current Q & A

Question / Comment	Answer / Response
[The question refers to the study by Professor Tzong-Lin Wu, National Taiwan University] Why are case 1 and 3 not different?	 Fig 1. case 1 Fig 2. case 2 Fig 3. case 3 Fig 4. case 4 In both case 1 and case 3, the trace is over solid copper (the voids are not directly under the signal path), and thus their EMI signatures are effectively the same since there is effectively no difference in the field behavior during propagation. In case 3, at certain frequencies, the plane may resonate based on the harmonics of the square wave. 

Could a designer route a return line, if it followed under the signal path? Would it need to be slightly wider than the signal line, or can it be the same width?	The fields on the trace do spread out a bit, but not by much, therefore, a slightly wider trace for the return path would be ideal. Keep in mind that the main purpose of using the routed return line is to have a return path for a low frequency signal rather than an entire plane. The return path could be routed on the same layer adjacent to the signal (this is called a coplanar wave guide). However, when the return path is routed adjacent to the signal, the field is not as well contained compared to having the return path below (or above) the signal trace. Note that the impedance will be a little more difficult to control when the signal and its return path are on different layers due to manufacturing tolerances.
What about triplets to a 5-line set, with gnd - signal1 - gnd - signal2 - gnd, so that gnd is on both sides of each of the two signal lines?	The 5-line set is acceptable; however, it is not required. Two signals can be side by side, as long as a ground is adjacent to each signal. Note that this use of triplets is not a perfect solution. This was done as a patch to contain signals on a board that was failing EMI. 
Are there any books you can recommend that provide more info? (See the list)	Rick has provided this list as a separate document. Please refer to the Nine Dot Connect's blog page for the list at https://www.ninedotconnects.com/blog/index.php/2018/08/02/rick-hartleys-reading-list/

Is there a need to split grounds for low noise analog circuitry? Can you speak further on the idea of not separating analog and digital ground planes?	The short answer – do not split the ground planes. Regardless of sensitivity, for low frequency analog circuitry (a few hundred hertz), the return fields will spread out. The reason why designers try to separate the analog plane from the digital plane is a 'concern' regarding the analog fields mixing with the digital. This 'concern' is unfounded since the return fields of the two signals types do not interfere with each other. For the higher frequency signals, the fields are contained directly under the signal (assuming that there is a plane or return path under it.) Nature likes to keep the volume of fields as small as possible. In addition, it also creates the path of least impedance. In short, the fields want to follow a low inductance, high capacitance path. For the analog, its wants to spread. Therefore, in an analog circuit, a signal trace running with a return line (as mentioned earlier) will be fine. What about sensitive circuits? The best way to handle it is to simply keep the analog in its area and the digital in its area. Avoid mixing the two signals. There is no reason to split the plane. Aside: In Rick's entire career, never once did he use a split ground plane. He simply isolated ground at very low frequencies.
With the 4-layer stack up with ground on both outer planes how do you attack components? Do you need to have a via next to every pad on every part?	The configuration does require a good deal of routing to be handled on the inner layers, thus the need for vias. However, for very small distances between components (lump length), they can be routed on the surface layers. The key question is, "What is considered a small distance?" This is defined based on the rise time. Consider Eric Bogatin's rule of thumb: If the trace is longer in inches than its rise time in nanoseconds, the line impedance must be controlled and terminated. For example, if the rise time is 1ns, the line should not be routed more than 1 inch on the outer layer. The route can be done if it does not 'terribly' disrupt the ground plane.
If using via fencing, are there issues when spacing the vias the same length?	As long as they are close enough together that the distance together is 'lump length' then there will be no resonances created by the their spacing. If the spacing is greater than a 1/10th wave length, then it is conceivable that one of the high frequency resonances of the signal could cause a resonance. If the distance is less than 1/10th the wave length is lumped length, it looks like solid wall of copper. When it comes to the spacing of vias, use the inner layer speed (which is slower). This will ensure that the spacing will accommodate both inner and outer signals.

In the 6-layer example, why have power for layer 2, rather than gnd, and have layers 1 and 3 be mix of signal and power, instead of being a mix of signal and ground?	<u>0.062" 6 Layer PCB Solution</u> ----Sig/Gnd----- -----Power------ **(Core)** ---- Sig/Gnd---- ---- Sig/Pwr----- **(Core)** -----Ground----- -----Sig/Pwr----- The primary benefit to this configuration is the use of 4 signal layers rather than three. Wherever you have the power layer, you also need ground for the signals as well. We are not trying to achieve high capacitance between power and ground planes; This can be achieved through a 1uf capacitor. Rather, low inductance is desired. Rather than a power plane, it is recommended that the board stack up be designed to have power planes available on all signal layers. Having pours around the board will make the routing a bit more difficult. However, if the effort is to keep the noise down, this is the better way to handle it.
What would happen if you took your 4-layer approach (grounds outside) in the 6-layer example?	If you put grounds on layers 1 and 6 and signals on 2 and 5, what is allocated to layers 3 and 4? If these are signal layers (which would be the primary purpose of going to a 6-layer board) this will result in 4 signal layers adjacent to each other internally. This would not be ideal for high speed design. There is a belief that ground pours must be placed on the outside layers because the ground pours will shield the signals from the world; however, striplines (inner layer lines) are typically quieter than the lines that are routed on external layers (microscrip). On outer layers, the cross talk is worse because of the greater spreading of the fields form side to side. As for containing fields, there is no difference between surface layer or inner layer. The only reason why the 4-layer board is recommended with grounds on the outer layers is to give more routing and power pours on the inner layers. Another recommendation for a 6-layer board is to have three routing layers: a ground on layer 1, routing and power on 2, Ground on 3, routing and power on 4, a ground on 5, routing and

	power on 6. This is preferred because it uses the prepreg layers for separation. This allows signals to be closer to the ground planes, as opposed to a larger distance between layers due to the typical core thickness. Note that this configuration can be reversed as well. <u>0.062" 6 Layer PCB Solution</u> ----Ground----- ----- Sig/Pwr ------ **(Core)** ---- Ground ---- ---- Sig/Pwr----- **(Core)** -----Ground----- -----Sig/Pwr----- Regardless, the downside to either configuration is the fact that there are only 3 routing layers.
In High speed design, can one get away with 4 layers?	It is very difficult. In the cost sensitive industries like auto and appliance, they will make it work to save costs. They are only going to consider another two layers if there is simply no other alternative. The two factors that benefit these cost sensitive industries: 1. The ability to lean on microcontrollers which are not as fast 2. The boards are not as dense. At some point the speeds and the densities are going to make a 4-layer board unviable. But in general, it is very difficult to do high speed in a 4-layer design because all the signals must be referenced to a plane.
Understanding return paths are especially important in switching power supplies.	When it comes to switching power supplies, it's not about how to set up ground; rather it's about component placement. What needs to be avoided is having a shared path between the feedback loop and the switchback loop. The high current of the switchback loop is going to corrupt the feedback loop. This will result in the circuit not functioning properly. There is no need to split ground. A good application note by Marty Brown - https://www.fairchildsemi.com/application-notes/AN/AN-1031.pdf

What is the Spacing vs Frequency requirements for via fence?	The “proper” answer is that the spacing must be no more than 1/10 of the wave length in the dielectric (dK). In the presentation, it was mentioned that the vias needed to be spaced at a 1/20th wave length of the frequency of the rising or falling edge. It is really all about the rising or falling edge, not about clock frequency, because the highest frequencies come from the rising and falling edges. Example: 500ps rising edge signal. Based on the formula .5/rise time for frequency, a 500 ps signal has an upper end frequency of 1GHz. The wavelength of 1GHz in free space is approximate 1 foot (~11.8 in) which also happen to be 300 millimeters. A 1/20th wave length is just under 6/10th of an inch. Therefore, the via spacing needs to be every 6/10 in (or 600 mils). They can be tighter, but they do not have to be. Another Example: 250ps signal rising edge signal, the calculation works out to the via spacing being every 300 mils. A rule of thumb: 1/10 of the wavelength in dK is approximately equal to the 1/20th in free space in FR4. Energy travels through FR4 at half the speed of light. Therefore, the 1/10 wavelength in dK is approximately equal to the 1/20th in free space. If the material is different, then the wavelength is the speed of light / Sq root dK, where dK is the dielectric constant. Beyond the rule of thumb, the ‘correct’ way of thinking is to think of it as 1/10th wavelength in the material itself because the wavelength will be shorter in the material than in free space. Its length is based on the dielectric constant of the board. The 1/20th wavelength is an approximate value.
Can you speak to the best way to apply Buried Capacitance (BC) to the stackups you've presented? Perhaps mention how BC could potentially help the last stackup (6-layer stack up) you presented?	Unfortunately, buried capacitors will not help the 6-layer stack up. First, it is very expensive. This is done on planes that are separate by no more than 2 mils. Applying 2 mil core to 6-layer board is extremely expensive fabrication effort. BC is used when dealing with very high layer count boards with very high frequencies. For example, a company in Sweden is using BC for a data network board that operates up to 32 Gigabit with 34 to 48 layers. They use the BC near the surface of the board where the ICs reside to get low impedance and low inductance planes to deliver power to the ICs.

Could you stick with the traditional stack-ups that you said were bad practice if you flood GND on the internal signal layers?	The objective of any stackup is to alternate between the power and ground to assist with power delivery. If there is a power plane and the signals are referencing the power plane, make sure that the pours on the signal layers are ground. If there is a ground plane, there shouldn't be ground pours on the signal layers because the intent is to reduce the inductance of the power/ground structure at high frequencies. Pouring grounds all over the place is not always the best solution. In analog, it makes sense to do so. In fact, in an analog board there is no reason to have a power plane, regardless of the frequency. Even on boards with 16GHz analog signals, routing power to the analog components was more than sufficient. The power can be routed because there is a resonant circuit at the IC that delivers clean power to the IC directly from that routed power line. Therefore, there is no reason have a "low impendence bus" for analog as one needs for digital. In short, in analog: route the power and provide ground; in digital alternate the power and ground layers.
Why do most IC manufacturers insist on separating grounds?	The applications engineers who work for IC companies understand circuit theory; but it is a completely different story when it comes to board layout because most AEs know little about the board layout issues. The prevailing philosophy – Split the grounds, for it is better to have something they know can be made to work rather than not split the plane and not have it work. IC companies are put in a bad spot when they tell the customer to do something, the customer does it, and the recommendation does not work. Therefore, they will take the most conservative approach. Another example – length matching – IC companies will tell the customer to match lengths within +/- 50 mil. However, this is more than adequate for a 10 Gigabit signal! However, you need to take their approach if you to expect them to respond if it does not work accordingly. The underlying issue – the IC company is only interested in the circuit functioning. When it comes to EMI testing, that is another story. Their concern – does the circuit function with their IC in it? Some of the advice is concerning – for example, they 'require' a split plane. As explained, is this necessary? And more so, this may introduce other issues if a trace crosses the plane or is run near the edge of the split plane.

Do you need to use other materials besides FR4 when dealing with high speed design?	Unless the circuit is operating higher than 3 to 4 Gigabits in a board no larger than 8 in, FR4 is perfectly fine to use. The reason – most (if not all) of the traces are going to be less than a foot long. If building a massive backplane where the lines are long and the frequency is high, that's the time to consider another material.
With the recommended 4-layer board, will high speed (several GHz signaling) be impacted by the via transition to layer 2 and then back to layer 1. In other words, is it worth routing on layer two vs the direction connection on layer 1.	As mentioned earlier, if a short trace can be routed on the top, it makes all the sense to do it. If the signal needs to be dropped to layer 2, the only time that there may be an impact on the signal is when the signal speeds exceed 10 Gigibits.
What can you do to combat bad chip designs?	Be vigilant and be vocal. If a chip is of interest, contact the IC manufacturer and ask to see the design of the substrate of the interpose board (this is the board that the chip is attached to.) It is good to know how the chip is attached to the substrate (ie, wire bonded, flip chip) since this will have an impact on the inductance. Just as important, look at the pin out for power and ground distribution. If the chip's power and ground distribution is not adequate as presented in the webinar, look at the competitor's chips. It also depends on the product. Microcontrollers lag in this area; however, high speed devices like microprocessors, FPGA and memories IC companies understand the need for speed and power/ground distribution.
Is there a substantial difference between a signal return on power vs gnd?	If routing a signal near power, it must be routed along the power that created it. For example, if the signal is 3.3V, it must reference the 3.3 power signal. Otherwise, it has no path for the return current to the driver. The result of the improper path is field spreading which will result in EMI issues. For sensitive signals, this can cause signal integrity issues. In addition, the power plane (or path) must be in close proximity to the ground plane to accommodate the fields. In short, be careful about using power as a return path.

If I hear correctly, you mention that the voltage creates the current? Is that correct?	Sort of. The voltage source (i.e, the power supply or battery) creates both the electrical and magnetic fields and the propagating energy is contained in the fields. It is the efficient propagation of these fields that is of most concern.
Biamp makes professional Audio equipment, mic/line preamps with 66dB gain, 10K impedance. We DO NOT split planes. And we never have trouble either.	Rick agrees completely! Do not split the planes!
If you have 2 traces that are far enough apart where there is a floating island of copper, how many vias should be placed?	If the purpose is to use it as a guard trace, place the vias so that the distance between the vias is less than 1/20th the wave length. If this cannot be done, it will be better to remove the island all together.
If applying a power source, isn't the power supply creating an electromotive force on the electrons to move them? By moving them, you are creating the fields. Doesn't the EMF of the power supply play a role?	Voltage and current are very important. With every voltage, there is an electric field. With every current, there is a magnetic field. Because of the way energy moves in the system and that the fields are in the dielectric, it is safe to say the energy moves in these fields.