"The accidental antenna and how to make one" Q & A

Comment / Question	Answer / Response
How do you get around DRC errors in F type antennas and differences in IPC netlist using Altium Designer? In particular, DRC shorts because the antenna copper is tied to the microstrip and ground?	When it comes to dealing with copper that must be shorted to other copper of a different net name, the best approach is to declare the component to be a 'net tie.'
What are some inexpensive ways to achieve the simulation visualizations like this webinar?	At this point in time, there really is not an inexpensive way because the 3D visualizations require field solving. There are very few programmers out there who can write code for this type of analysis. In addition, the sheer number of calculations requires hardware that can access multiple cores for processing and can access a great deal of memory.
Does the effectiveness of using a power plane as a reference plane depend on the number and proximity of bypass capacitors?	Yes, the frequency of operations dictates the number and placement of the bypass capacitors.
Should you use stitching capacitors symmetrically for the strip line?	If you have room in your layout, it is the best approach.
Given a reference plane and strip lines, what is the effect of stitching the top ground to the reference plane?	The top ground plane helps reduce the radiation and impact of having a slot.
Can we use two words in multiple reference planes earth, ground, DC+ voltage and reference? [The question is referencing the ability or inability to represent a net using different words]	The signal will not care what you use as a reference plane so long as they are tied together via stitching capacitors
Given a reference plane and strip lines, what is the effect of stitching the top ground to the reference plane on coplanar waveguides?	We can model the specific structure in HFSS as to show the frequency dependence of the transmission line and any discontinuities.

What's the name of the GNU tool?	Look up GNU plot. Keep in mind that it was created for UNIX back in the 1980s. You may have to use a Linux system to make use of it.
In any reference plane there are typically vias that create slots. How close can vias be placed to microstrips?	I try to keep any primitive belonging to a different net at least 2H (H = dielectric height) away. 3H is better. 1H is a minimum.
How far out from the microstrip edge does the side energy of the reference plane extend?	Typically, two or three dielectric thicknesses away from the edge of the microstrip line.