Practical Aspects of Signal Integrity Q & A

Question / Comment	Answer / Response
What type of mathematical model does the Cadence Sigrity tool use?	S-Parameters, IBIS, and SPICE models
What is a slow rise time that causes Signal Integrity?	Depends on your design. Slow rise times typically don't cause signal integrity issues.
Is the transmission line at 50 ohms? Is the 40 ohms on-chip a series resistance?	Transmission lines can be any impedance. 50 ohms is the standard for cables and such, but for high-speed devices on a PCB it can be whatever works. For example, USB is 90 ohms, and DDR uses anything from 30-60 ohms. ODT is a complicated topic, using switched series and parallel resistances to fine-tune the impedance.
The bend types help with EMC, when do you use the appropriate bend for EMC?	As shown in the examples, bends have very little effect on signal propagation. Ultimately the issue with bends comes done to the change in impedance that is created by the bend and the impact that causes. Only on a case-by-case basis can one determine if that impact is significant enough to warrant the need for implementing special bending of traces from 90 degree turns.
Why would you change the impedance of the trace when it is matched?	When routing constraints prevent you from keeping the same trace width. For example when needing to route between the pads of a BGA package you will often need to "neck down" the trace to a thinner width.
At a high frequency is it necessary to have multiple grounds or a single point ground is okay?	The field of Signal Integrity does not use the word "Ground"! You want a clean signal reference path, typically a copper plane. Having many connections to this plane helps ensure small inductance loops.
Why wasn't Altium used for SI? Can it be used for SI?	Altium seems to use an equation-based analysis which is insufficient to handle the complicated electric and magnetic field modeling (known as "field solvers") needed for true Signal Integrity analysis.
How does the Altium 19 Signal Integrity tool compare to the Cadence tools used in this webinar?	Altium doesn't provide field solver SI simulation.

We deal with high voltage, 2KV-8KV voltages and high currents of 100A - 600A so signal/power integrity is a major issue. Can you address those issues?	Obviously the higher voltage requires greater separation which only helps with reducing crosstalk. However, since it is the di/dt that is involved with the coupling of signals and with very high currents that di/dt problem is complicated for the same time interval, then the extra spacing is probably negated. Again, any situation that is outside of normal/typical signal paths really needs 3D simulations to accurately assess the situation in order to evaluate if any issues are present.
I have a controlled impedance video diff pair that also contains series resistors, series capacitors and protection diodes. What do all these components do for the matched impedance of the signal	Anything that changes the dimensions of a trace will affect its impedance for the worse. Adding in components and their SMT pads will cause impedance mismatches, no matter what the device. To determine the actual effects, a full simulation would be needed.
Termination is for?	We will address termination schemes in Part 2 of the webinar series.
With trace width (impedance) changes, does the length of the non-ideal width or the number of transitions have a larger affect?	It is the change in impedance that usually causes problems due to reflections. So the number of changes will typically have more of an effect. How about this: each change of impedance causes reflections. Therefore, the more changes you have, the more ripple is created because of the interactions of each reflection with previous reflections.
Is a single point ground better at high frequency then multiple grounds for SI?	Do not confuse single-point grounds for the purposes of noise control with the use of reference planes for high-speed signal integrity concerns. They are two different aspects of design. When routing signals and a change in layers is needed, you are better off to have multiple vias in order to maintain a more balanced approach of field behavior through the transition. Remember that the role of vias in SI is to help contain fields in a manner that is conducive to the most efficient propagation between source and load. Any distortion of that field results in coupling and/or radiation.