Translation Checklist

The following checklist is a general guidance for design cleanup after importing a design from another EDA tool. Some of it is more Altium related, but the procedure would be similar if using a different EDA tool. One must be proficient in the tool being used. The actions that need to be taken will differ from those used for a new design.

	Action Item	Purpose / Notes
1	Check designator annotations between schematic and PCB; check component links	In a netlist, the component designators provide the relationship between the schematic symbols in the PCB footprint. If the annotations were changed in the PCB and have not been back annotated, it will be extremely difficult to reconcile the differences between the schematic and the PCB after it has been imported. Ensure that there is a unique ID assigned to both the schematic symbol and the PCB footprint for each component as well.
2	Make a footprint and schematic library	This simply captures the components that were used in the project. Additional cleanup of the library will more than likely be required.
3	Move all PCB primitives if in a location that is not readily accessible in the editor	In many cases, the imported PCB with all of its primitives will be placed at the absolute origin of the PCB editor. This will make it difficult to edit anything below the bottom edge of the board.
4	Turn off the Design Rule Checker (DRC)	When the board is first imported into the PCB editor, there will be numerous DRC errors. Though these will be addressed in the later part of this procedure, there are other priorities that need to be handled prior to cleaning up these errors.
5	Check layer stack	Review the layer stack to determine which layers were used for signals and planes. This may not be obvious with certain boards that may have taken liberties with polygon pours as needed.
6	Preliminary mechanical layer cleanup	There will be a number of various mechanical layers that have been imported that do not contain any information pertinent to creating manufacturing files. In some cases, other features of the EDA tools may be able to assist, rather than placing them on mechanical layers. The more primitives that are present in the PCB editor the more time needed for the tool to make changes. Therefore, remove what can be removed.

7	Resolve signal continuity issues	Though the DRC online checker may be disabled, this does not mean that one cannot see the discontinuities in the signals. Make sure that the connection lines (rat's nests) are enabled. In many cases, the discontinuities will be due to issues with the polygon pours. These will need to be resolved. This may also require comparing of the Gerber files. This will allow the user to see if the rules driving the polygon pours need to be adjusted so that the continuity will be complete.
8	Clean up the DRC	Once all net connections in the PCB have been resolved, enable the online DRC to determine which rules need to be modified. Remember that the PCB, if it has already been manufactured, should have rules that result in Gerbers matching the original manufacturing files.
9	Begin schematic to PCB reconciliation	Once the PCB is error-free and all continuity has been re-established, it is now time to link the PCB to the schematic. In a translation, the PCB is the driving document. This is different from the traditional design process in which the schematic drives the PCB. There are several things that need to be done:
9a	Electrical Rule Checker (ERC)	Run the ERC to see if there are any translation issues that need to be addressed. In some cases, this could be shorts due to a net label shorting out two lines or it could be a conflict of net labels between a power symbol and a net label. All ERC errors and warnings should be reviewed and either fixed or justified.
9b	ECO Between PCB and Schematic	Run the ECO between the schematic and the PCB. Review all existing issues. Do not push anything from the schematic to the PCB since the PCB is the master document when translating a design. Any changes that need to be done should be done in the schematic. This may include the declaration of differential pairs, net name changes, and footprint link modifications, etc.

10	Schematic cleanup	Schematic cleanup is generally in the form of changing fonts on text and converting all off-sheet connectors to ports. All schematic files should be reviewed to make sure that there are no net labels that are shorting two wires together. This also includes any symbol cleanup of the pin labels, etc.
10a	Generate bill of materials from both the schematic and the PCB	If footprint differences were detected between the schematic and the PCB, generate a bill of materials from both the schematic editor and the PCB editor to determine which footprints are being declared on each side. Remember that the PCB document is the driving document.
11	Modify libraries	If concerns are found in the PCB footprint names, make sure that the original footprint names are kept and the schematic and PCB are in sync with each other prior to making any new footprint names. These will have to be resolved in the schematic library, the schematics, and the PCB. In addition, this would be the time to clean up any mechanical layer issues and to add 3D footprints.
12	Generate manufacturing documents	Generate all manufacturing documents as one would do with any needed design. If using another manufacturing format such as ODB++ or the IPC 2581, generate Gerber files as well.
13	Compare final Gerbers	Compare the new Gerbers against the original documentation. All aspects of the new Gerbers and the old Gerbers should match up verbatim: Etch Solder Paste Solder Mask Silk